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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/09/07	Deciphered Date	2014/09/07	BLOCK DIAGRAM	
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane State	B+	+1VALW +1.8VALW +3VALW +5VALW	+1.35V	+5VS +3VS +0.675VS +VCC_CORE +VGA_CORE +3VS_VGA +1.8VS_VGA +1.35VS_VGA +1VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON	SUSP#
S0		HIGH	HIGH	HIGH	HIGH	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF

USB2 Port

Port	Device
1	On Board
2	On Board
3	SUB/B
4	ONE-Link DOCK
5	Touch Panel
6	BT
7	CMOS
8	FPR
9	X

USB3 Port

Port	Device
1	On Board
2	On Board
3	SUB/B
4	ONE-Link DOCK

PCIE Port

Port	Device
1	X
2	X
3	WLAN
4	LAN
5	X
6	CardReader
7	X
8	X
9	GPU
10	GPU
11	GPU
12	GPU


SATA Port

Port	Device
1	HDD
2	X
3	X
4	X

SMBUS Control Table

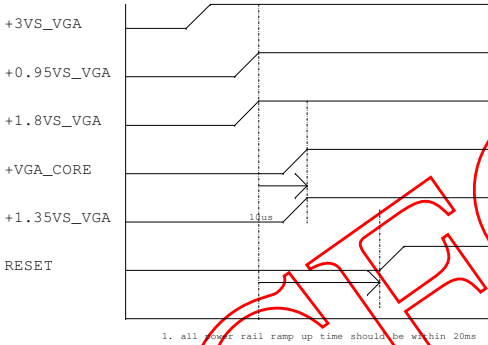
	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY	G-Sensor
EC_SMB_CLK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CLK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3VALW_PCH	X	X	X	V +3VALW
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	V +3VS	X	X	X	V +5VS	V +3VS	X	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3VALW_PCH	X	X	X	X	X	X	X	X	V +3VALW	X

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VGA and DDR3 Voltage Rails (JET TOPAZ GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN	-	GPIO5_AC_BATT
GPIO6	IN	-	GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	-	GPIO8_ROMSO
GPIO9	OUT	-	GPIO9_ROMSI
GPIO10	OUT	-	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN	N/A	SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN	IN	SVI2_SVC
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	

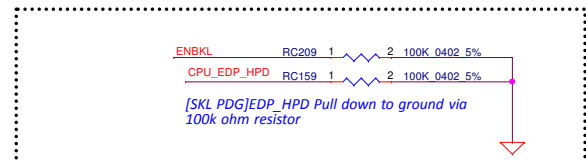
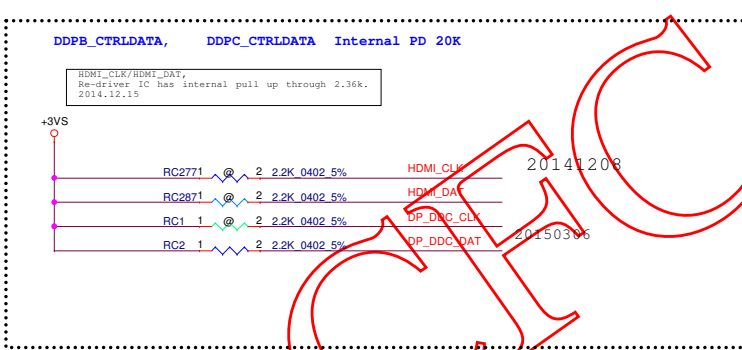
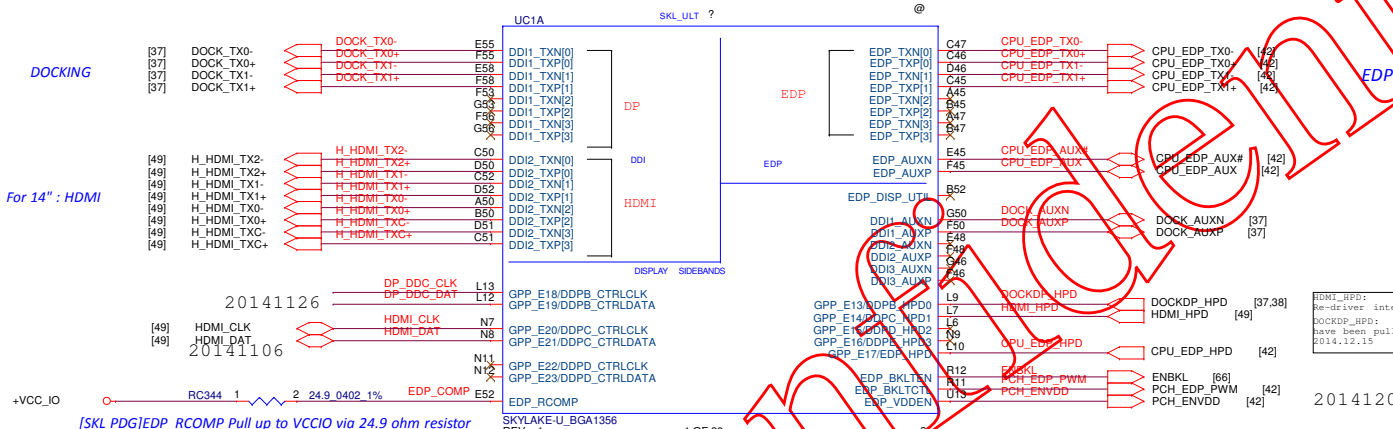


	Device ID
JET-XT	0x6664
TOPAZ XT	0x6900

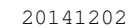
BOM Structure Table

BOM Structure	NOTE
EXO@	For GPU_EXO
MESO@	For GPU_MESO
DIS@	For GPU function
X76@	GPU VRAM Setting
TPM@	Trusted Platform Module (TPM)
DIMM1@	JDIMM1 function
DIMM2@	JDIMM2 function
UMA@	UMA SKU ID
DPRE@	DP re-driver function
NODPRE@	Disable DP re-driver
MIRROR@	For mirror function
ME@	ME Connector
EMC@	For EMC function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
U31@	For U3 port1 redriver function
U32@	For U3 port2 redriver function
U33@	For U3 port3 redriver function
NU3R@	No U3 redriver function (All port)
RF@	For RF function
TS@	For Touch function


			RV104	RV105
Memory (GDDR3)				
Samsung	1G	SA22225SH30*4	PU 8.45K	PD 2K
	2G	SA000063F00*4	PU 3.4K	PD 10K
Hynix	1G	SA00005VS10*4	PU 4.53K	PD 2K
	2G	SA00005YL10*4	PU 4.75K	NC
Micron	1G	SA00005M100*4	NC	PD 4.75K
	2G	SA000060I00*4	PU 3.24K	PD 5.62K



DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20 K Ω nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 K Ω \pm 5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20 K Ω nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 K Ω \pm 5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.



[SKL PDG]DDR_RCOMP
1. Trace width=12~15 mils, Spacing=20mil, Max length=500mils
2. R close to MCP

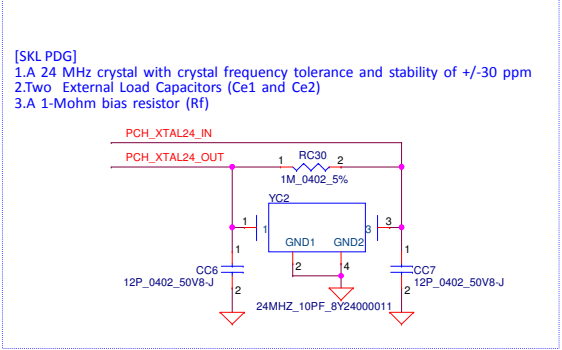
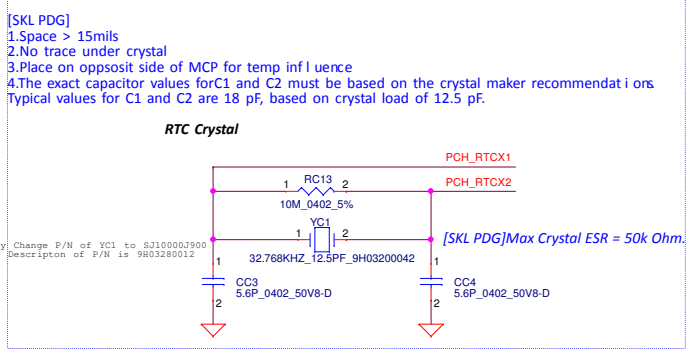
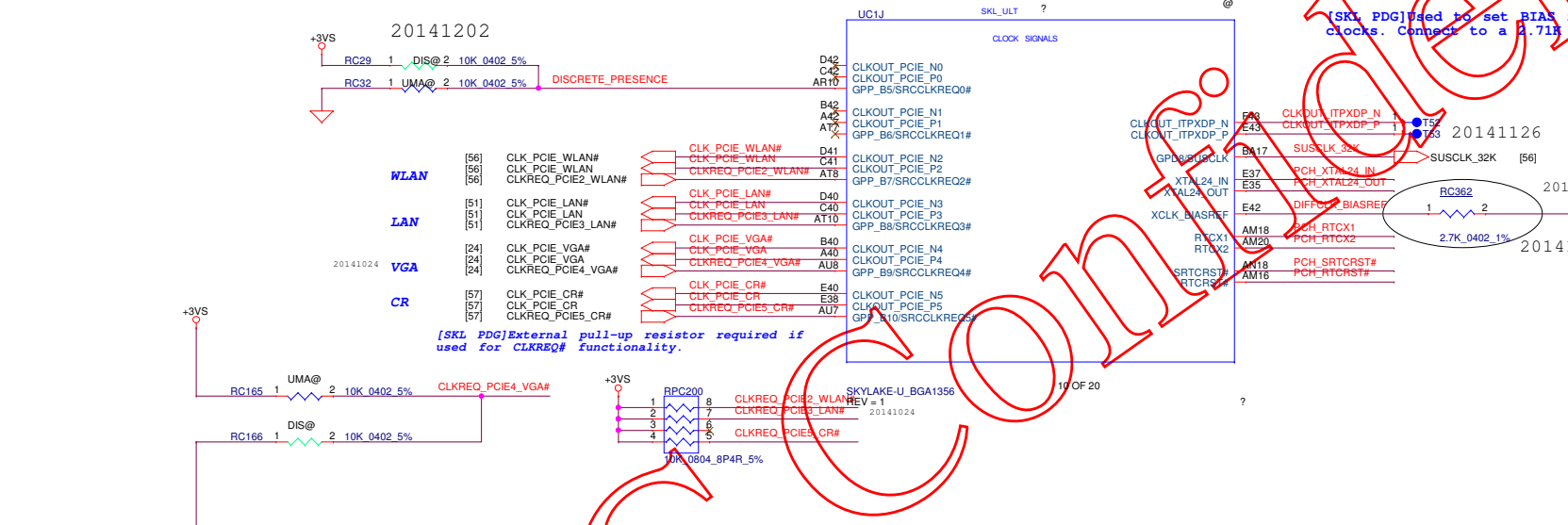
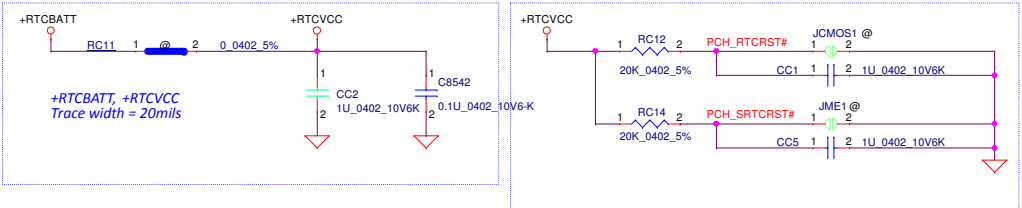


551

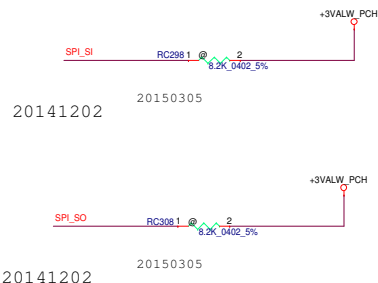
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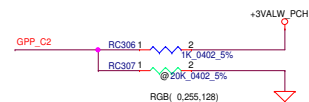
RTC External Circuit



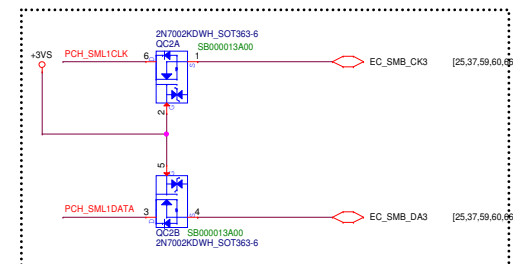
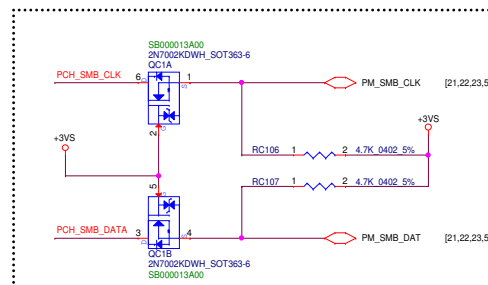
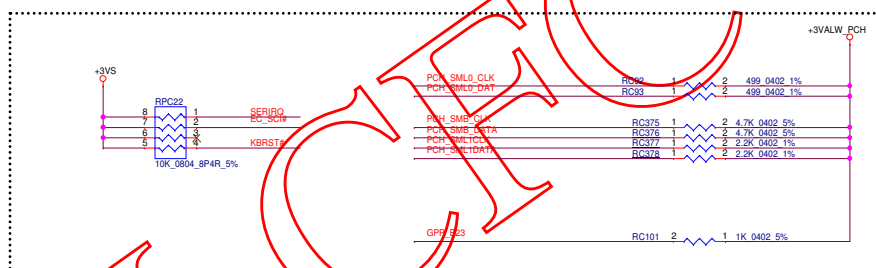
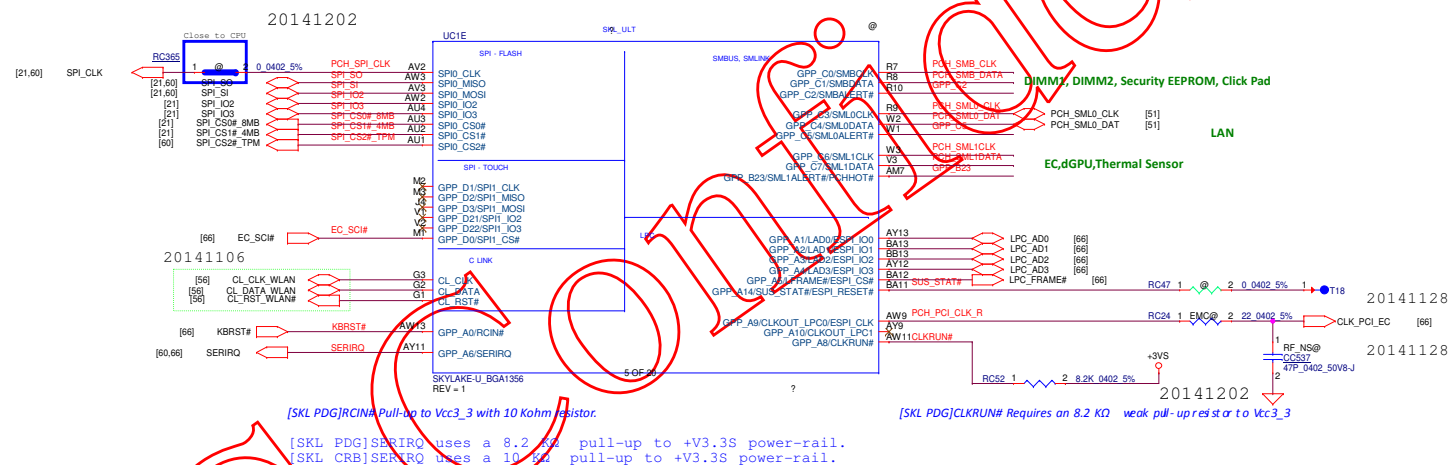
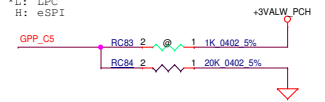
This signal has an internal pull-up.
This strap should sample HIGH. There should NOT be any
on-board device driving it to opposite direction during
strap sampling.




```
L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher
suite (with confidentiality).Support Intel AMT with TLS and Intel
SBA (Small Business Advantage) with TLS.
```



```
*L:  LPC
    H:  eSPI
```



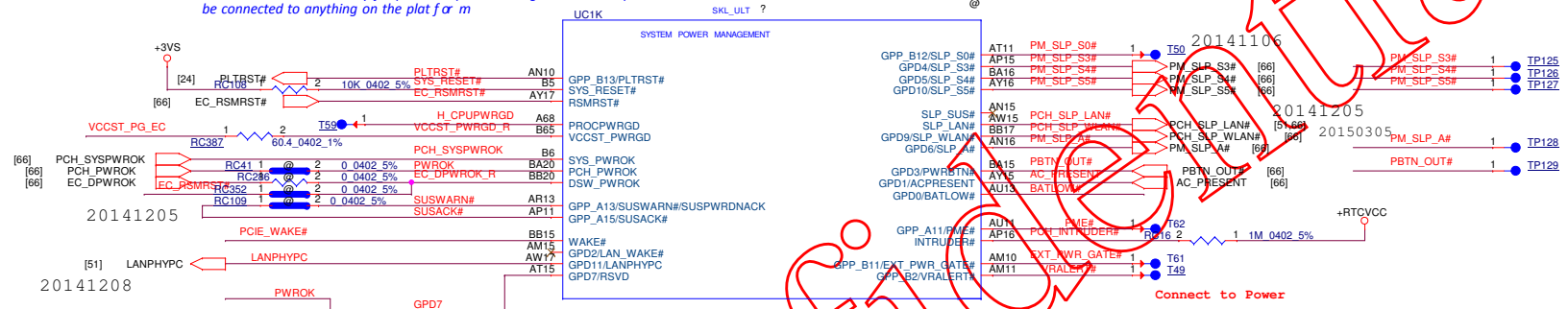
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Issued Date		2014/05/07		Deciphered Date		2015/05/07		SKL(7/16):LPC/SP/SMBS/CL		
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[SKL PDG]SYS_RESET#: Connect this signal on PCH directly to the reset button and pull-up to +V3 3Vcc external through a weak pull-up resistor (8.2~10 Kohm).

[SKL PDG]PROCPWRGD
1. Indicates that VCCIN, VDDQ power supplies and clocks are stable. This signal will be asserted only after PCH_PWROK assertion.
2. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.

[SKL PDG]SLP_S3, SLP_S4, SLP_S5 No pull-up/pull-down resistors needed. Signals driven by the PCH.

[SKL PDG]SLP_A: No pull-up/pull-down resistors needed. Signals driven by the PCH. Can be left as NC when the Intel Management Engine (Intel ME) is not supported on the platform. When asserted (Intel R_Me is not supported).



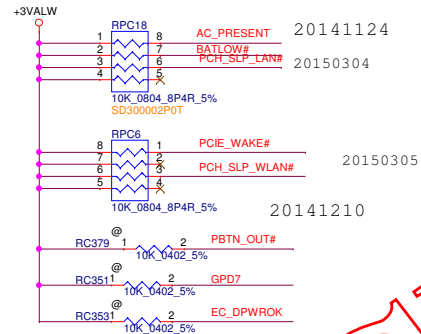
[SKL PDG]AC_PRESENT: 8.2~10 K Ω pull-up to DS Wvdl.

[SKL PDG]BATLOW#: 8.2~10 K Ω pull-up to DS Wvdl.

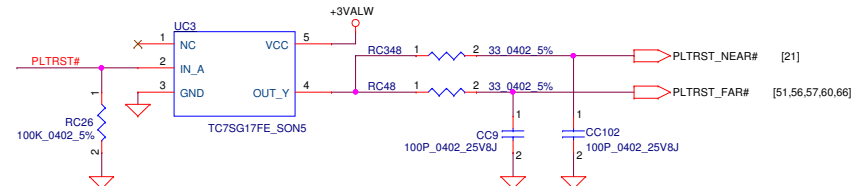
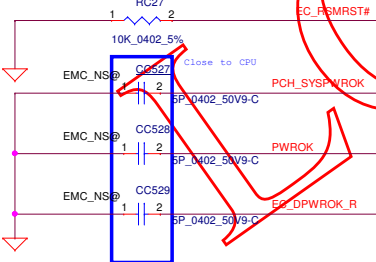
[SKL PDG]WAKE#: 10 K Ω pull-up to Vcc DS V3_3

[SKL PDG]APWROK: There is no corresponding APWROK signal input to the PCH, but the PCH does have an internally generated version of APWROK that is tied to mSLP_A#.

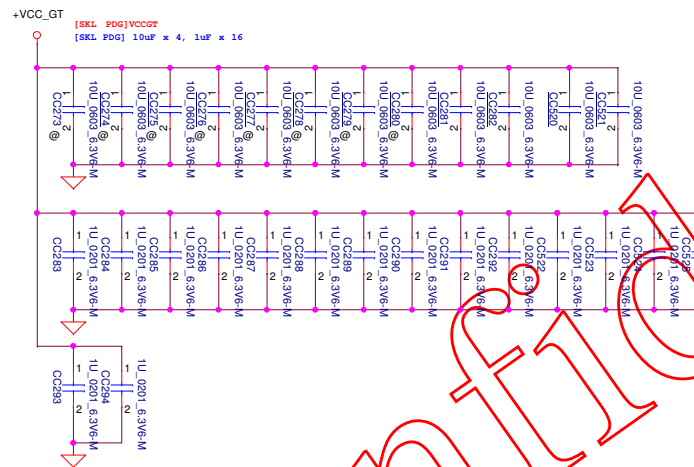
[SKL PDG]EXT_PWR_GATE# (External Power Gate)
1. HSIO Power Control: Used to control power to VCCMPHYGT_1p0, VCCMPHYPLL_1p0 and VCCSRAM_1p0 in S0 & Sx.
2. PCH will drive EXT_PWR_GATE# low when all the high speed IO controllers (xHCI, SATA and PCIe) are idle or have no devices attached.




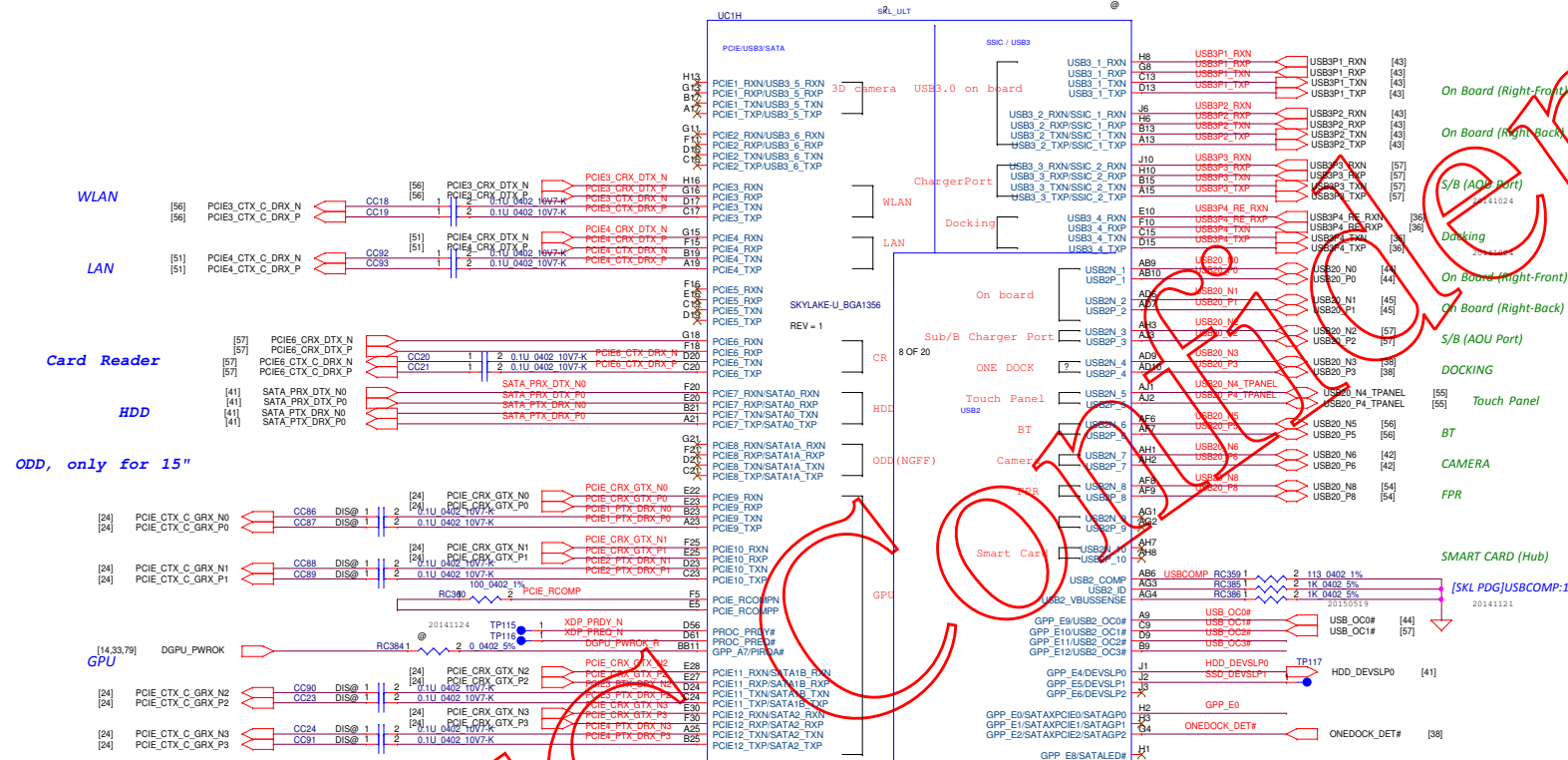
[SKL PDG]RSMRST#: Recommend an 8.2~10 Kohm pull-down resistor to ground.
Note: CRB uses 10 K Ω pull-down.



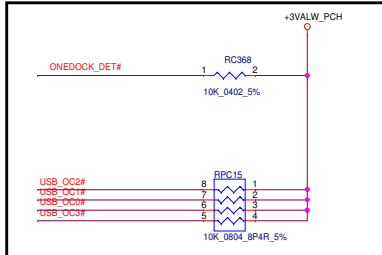
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Issued Date				Deciphered Date				SKL(8/16):SYSTEM PM		1.0	
2014/05/07				2015/05/07				Size Document Number		BB460 NW-A551	
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USB_OC0#	Port 0, Port1
USB_OC1#	Port 2, Port3
USB_OC2#	Port 4, Port5
USB_OC3#	Port 6, Port7



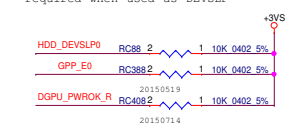
[SKL PDG]PCIE_RCOMP
1.100 ohm +/-0.1% external resistor between RCOMP/RCOMPN

2.SATA compensation circuit is code share with
PCIE_RCOMP/N differential pair. Refer to RD Express
Design Guidelines chapter for PCIE_RCOMP/N guideline.

3.Width:12~15Mil
Space>124Mil
Length:Both RCOMP & RCOMPN need to matched to less than 1% trace and board

[SKL PDG] OC [x] pins require a pull-up to VccSus3_3 with 8.2~10 Kohm resistors

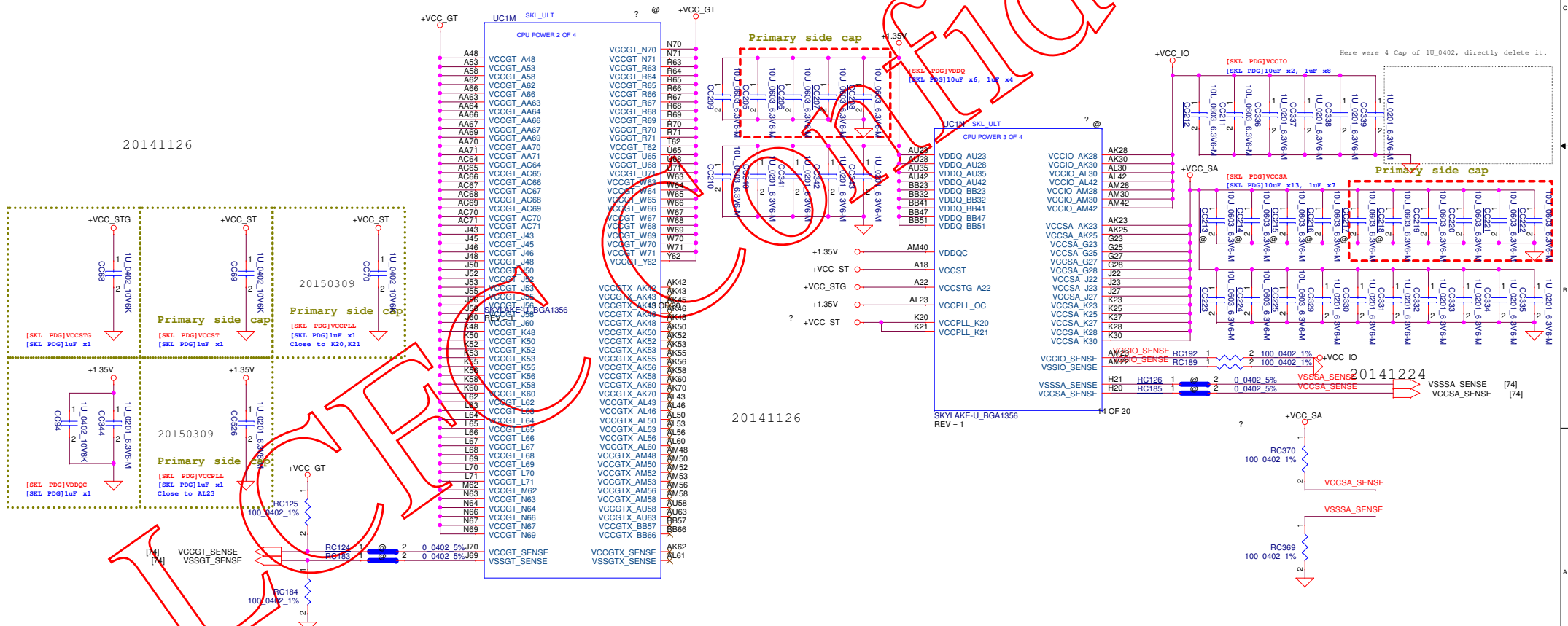
[SKL PCH EDS]no external pull-up or pull-down termination
required when used as DEVSLP

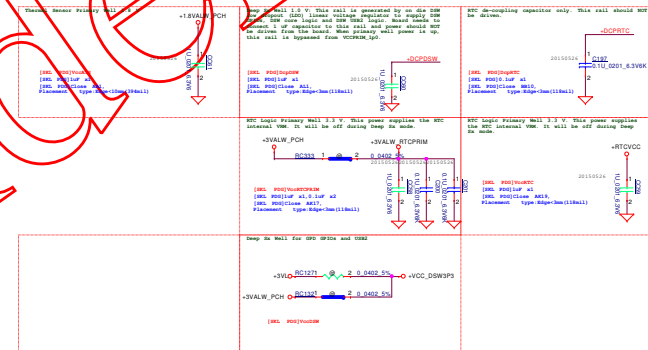
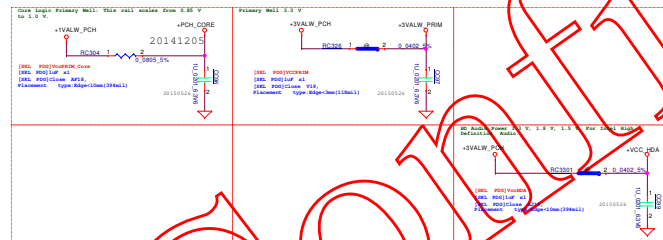
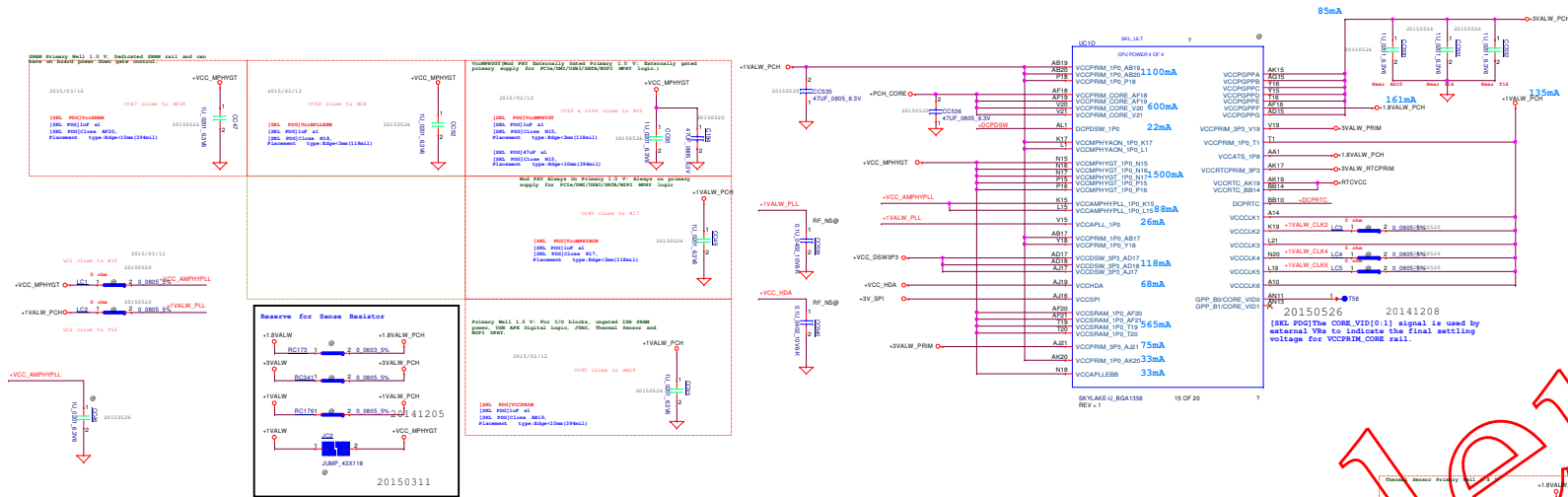




[SKL PDDG]Package Sensing Recommendations

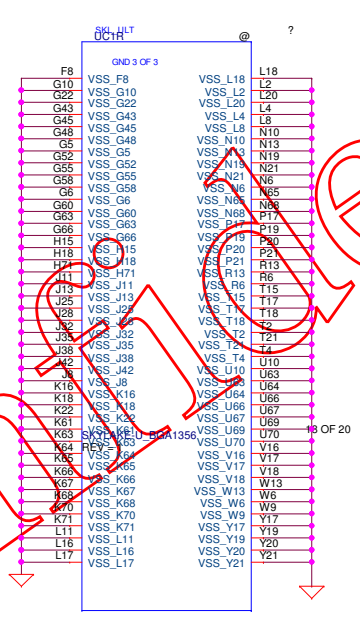
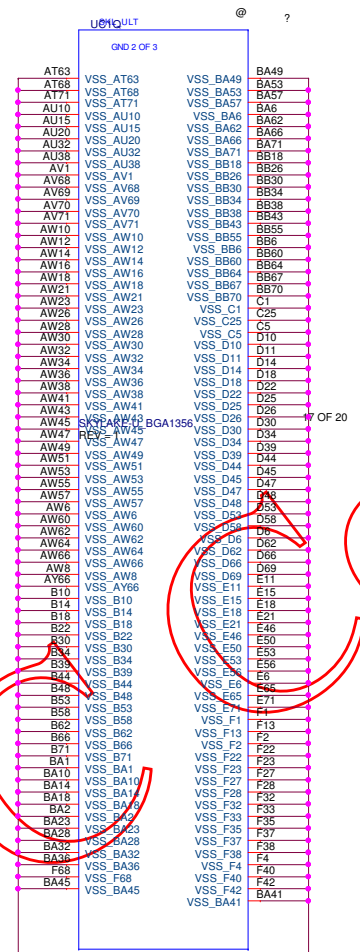
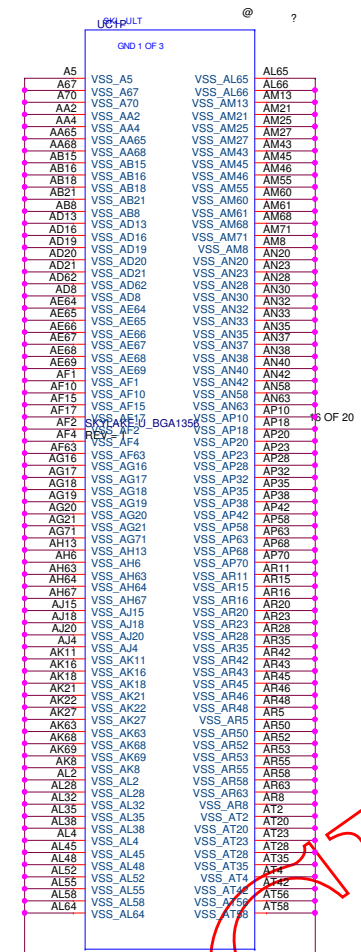
1.Alert signal must be routed between Clk and Data signals to minimize Cross-Talk.



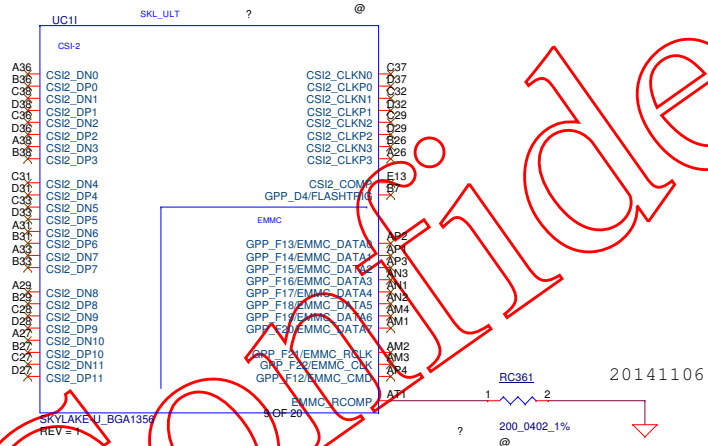


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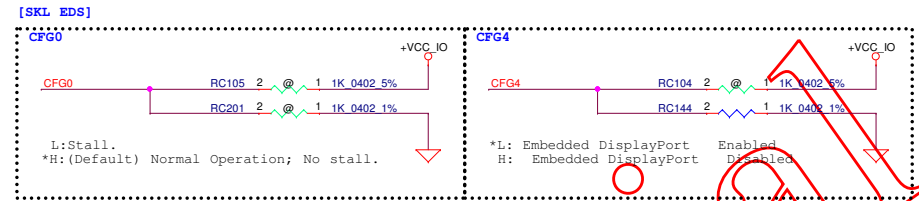
Security Classification		LC Future Center Secret Data		Title	
Issued Date		Discontinued Date		SKL(13/16)-POWER	
20140507		20150507		RE100-NH-A551	
Rev D		Rev 14		17 of 18	



LCFC CONFIDENTIAL



20150309
(Test point change to 12mil)



TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled

[SKL EDS]Zero Voltage Mode:VCCOPC is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

ZVM#	state	VCCOPC
0V		0V
1V		1V

[SKL EDS]Minimum Speed Mode: VCCEPIO can be connected to OPC VR in this case VCCEPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal. In order to achieve better power/performance it is recommended to use a separate VR for VCCEPIO in this case VCCEPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EPIO interface as shown below:

ZVM#	state	MSM#	state	VCCEPIO
0V		X		0V
1V		0V		0.8V
1V		1V		1V

[SKL CRB]

+1VALW_PCH RC152 2 1 49.9 0402 1%
RC354 2 1 1.5K 0402 5%
ITP_PMODE
Termination: Resistor value from 1K ohm to 3K ohm pull up to PCH_V1.0A Rail.

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20141202

[SKL CRB]

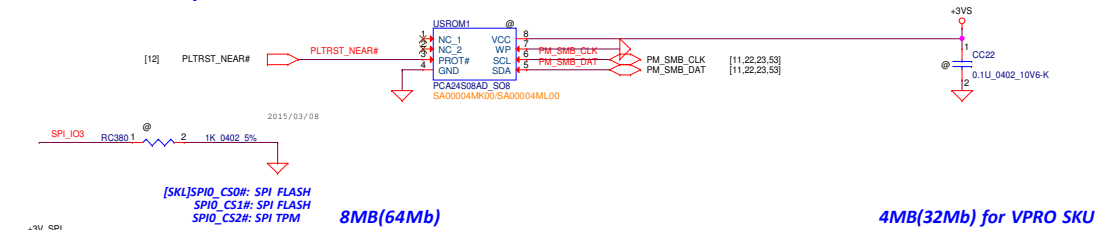
UC1T SKL_ULT

SPARE

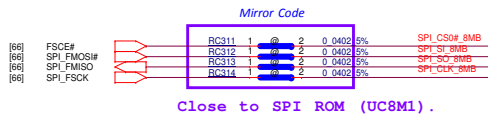
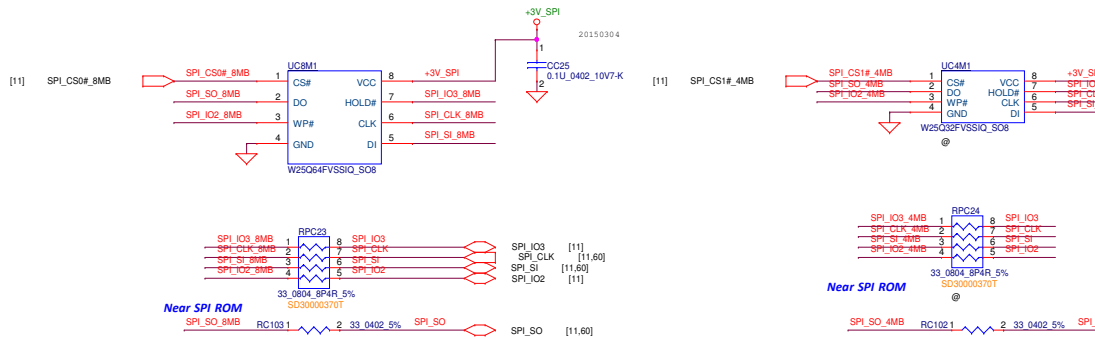
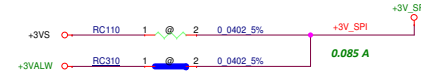
SKYLAKE-U_BGA1356
REV = 1

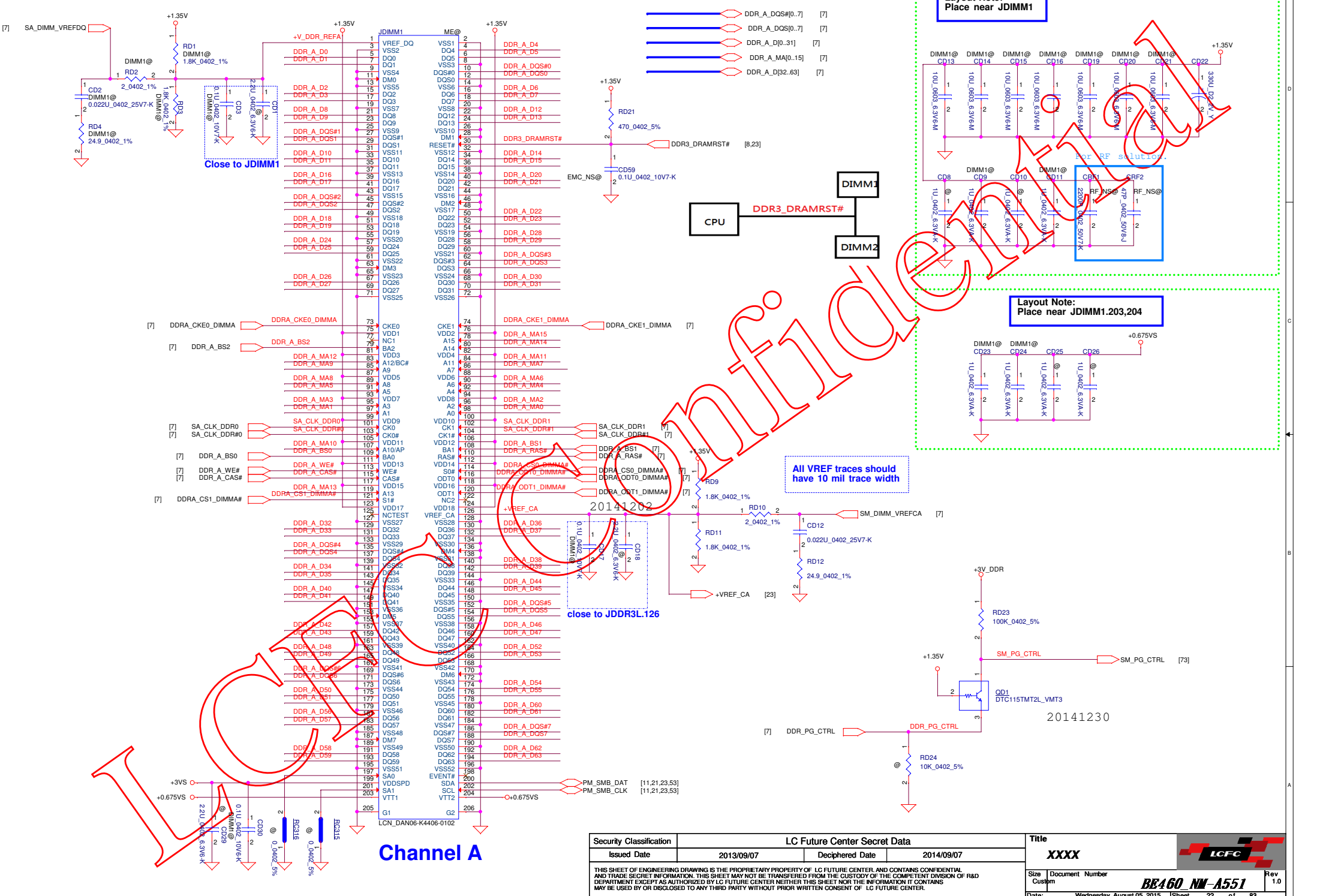
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Security ROM



M3 Support + Intel LAN PHY / Wireless LAN Solution






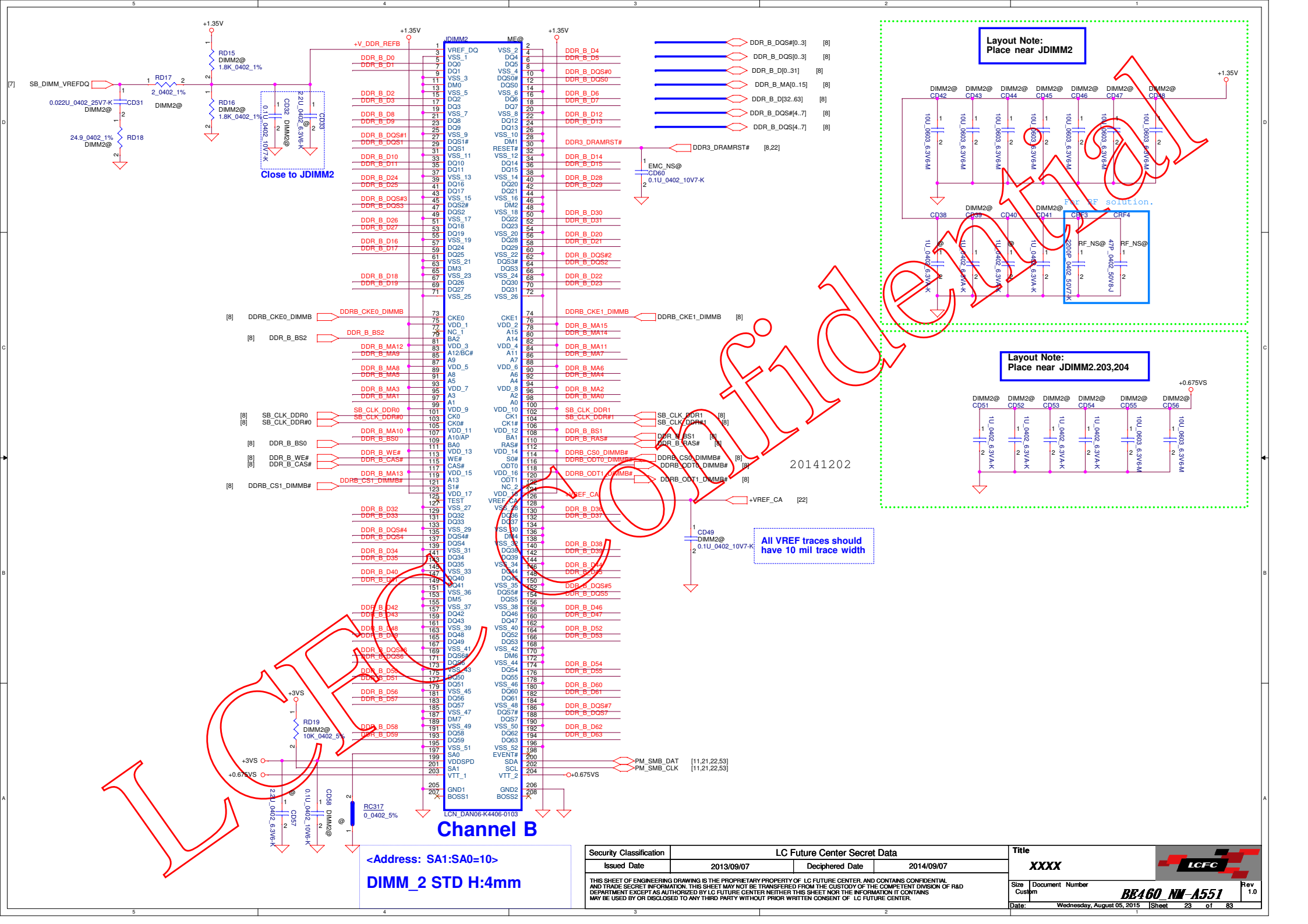
Layout Note:
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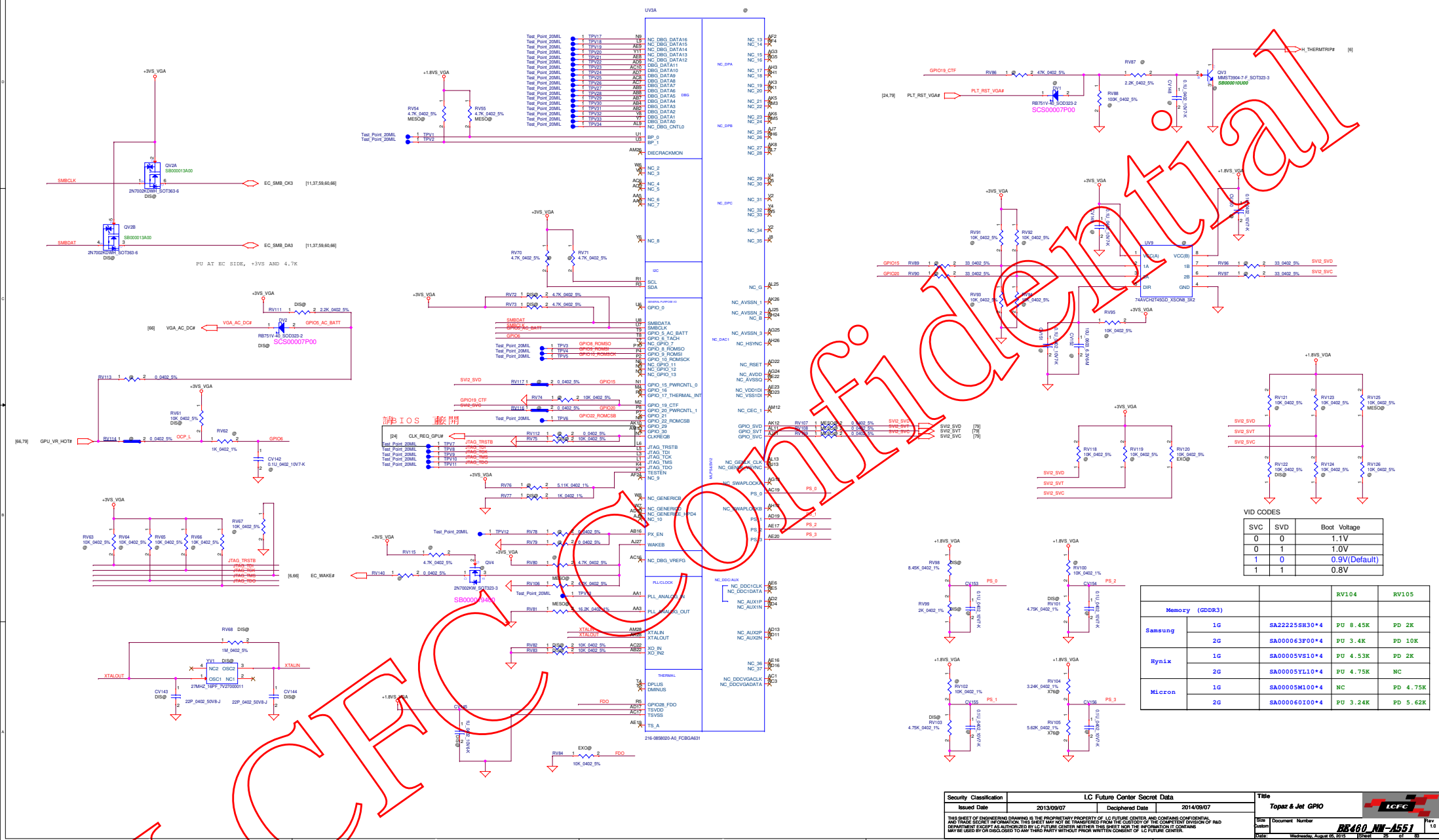
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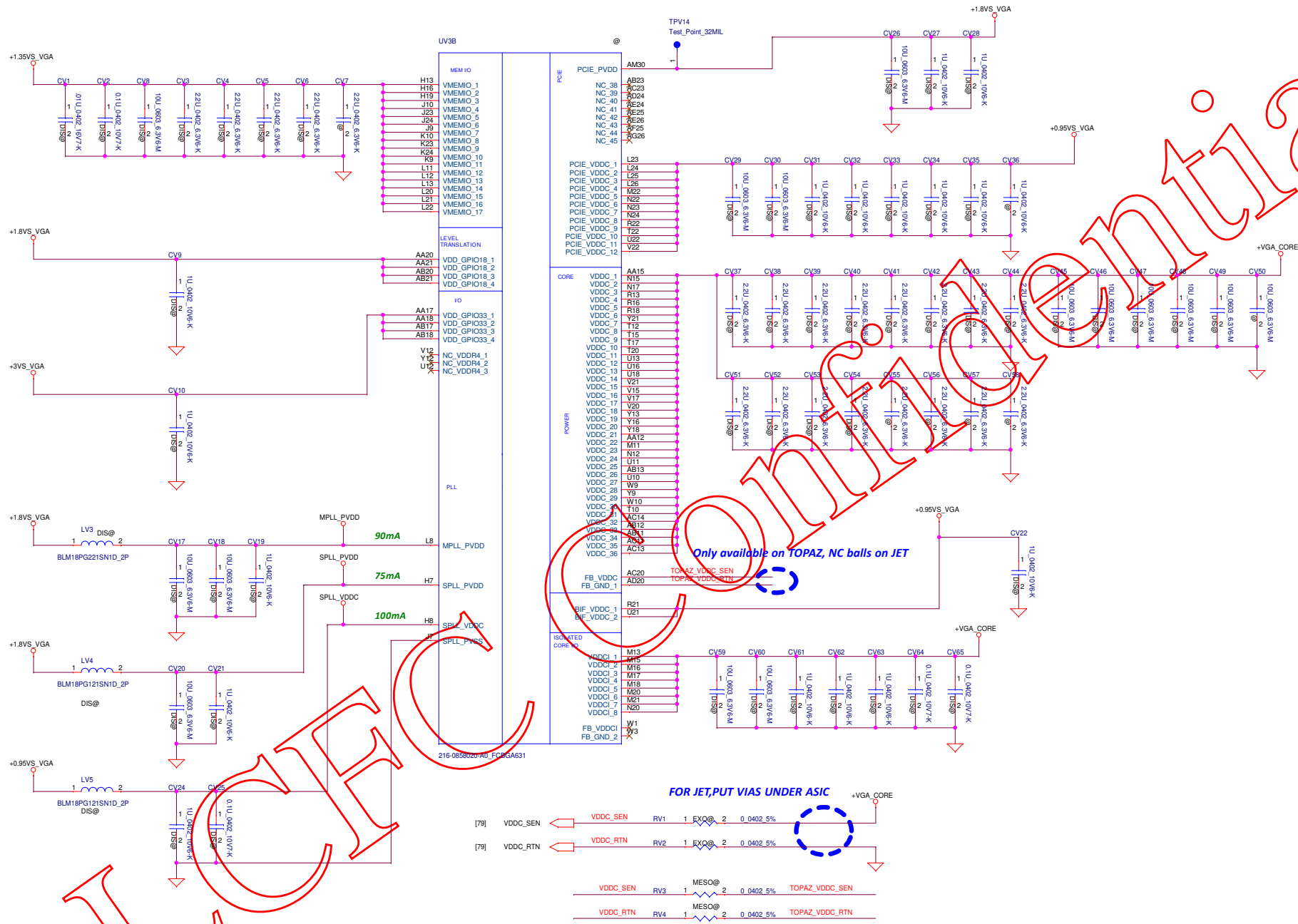
All VREF traces should
have 10 mil trace width

Channel A

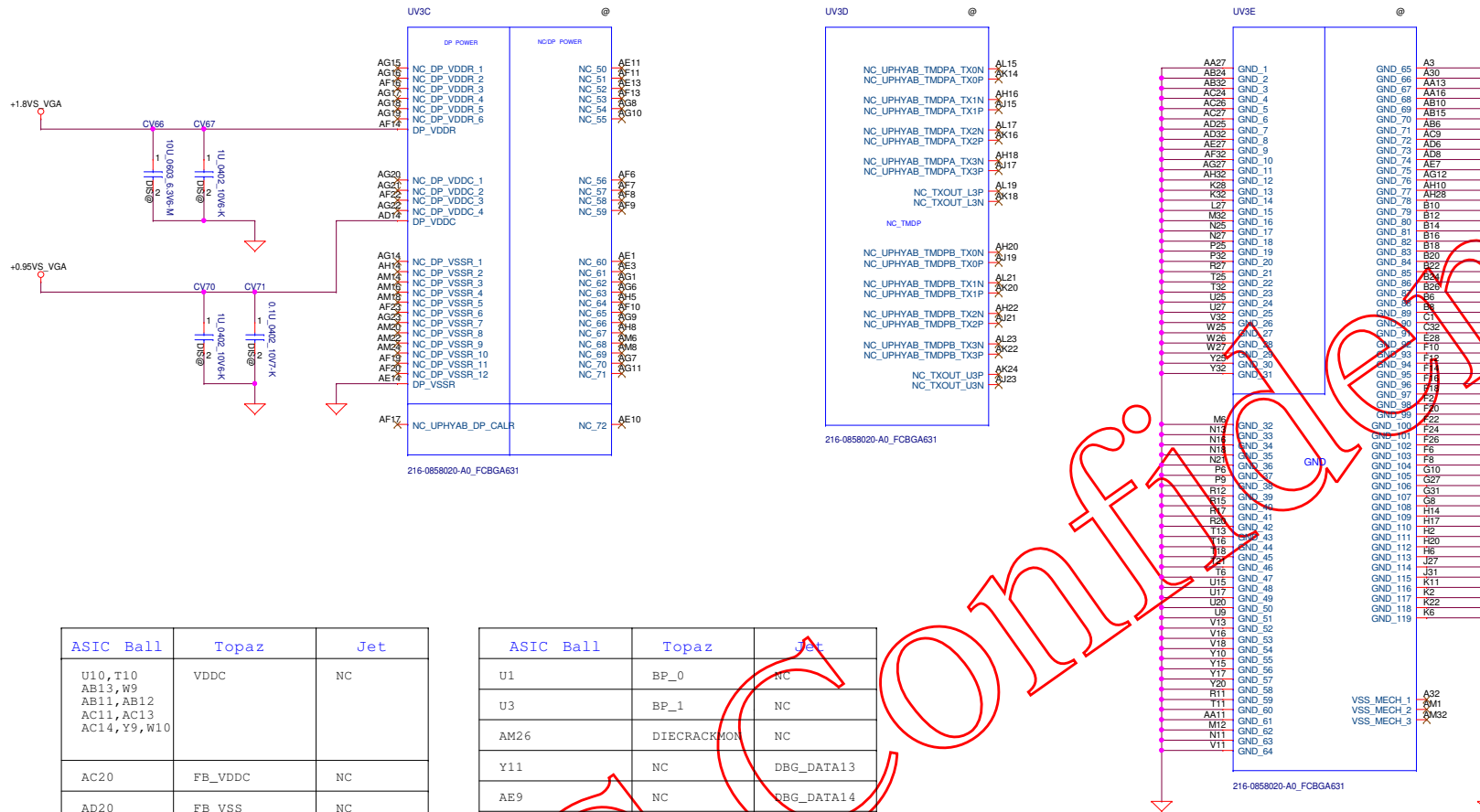
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Custom					1.0
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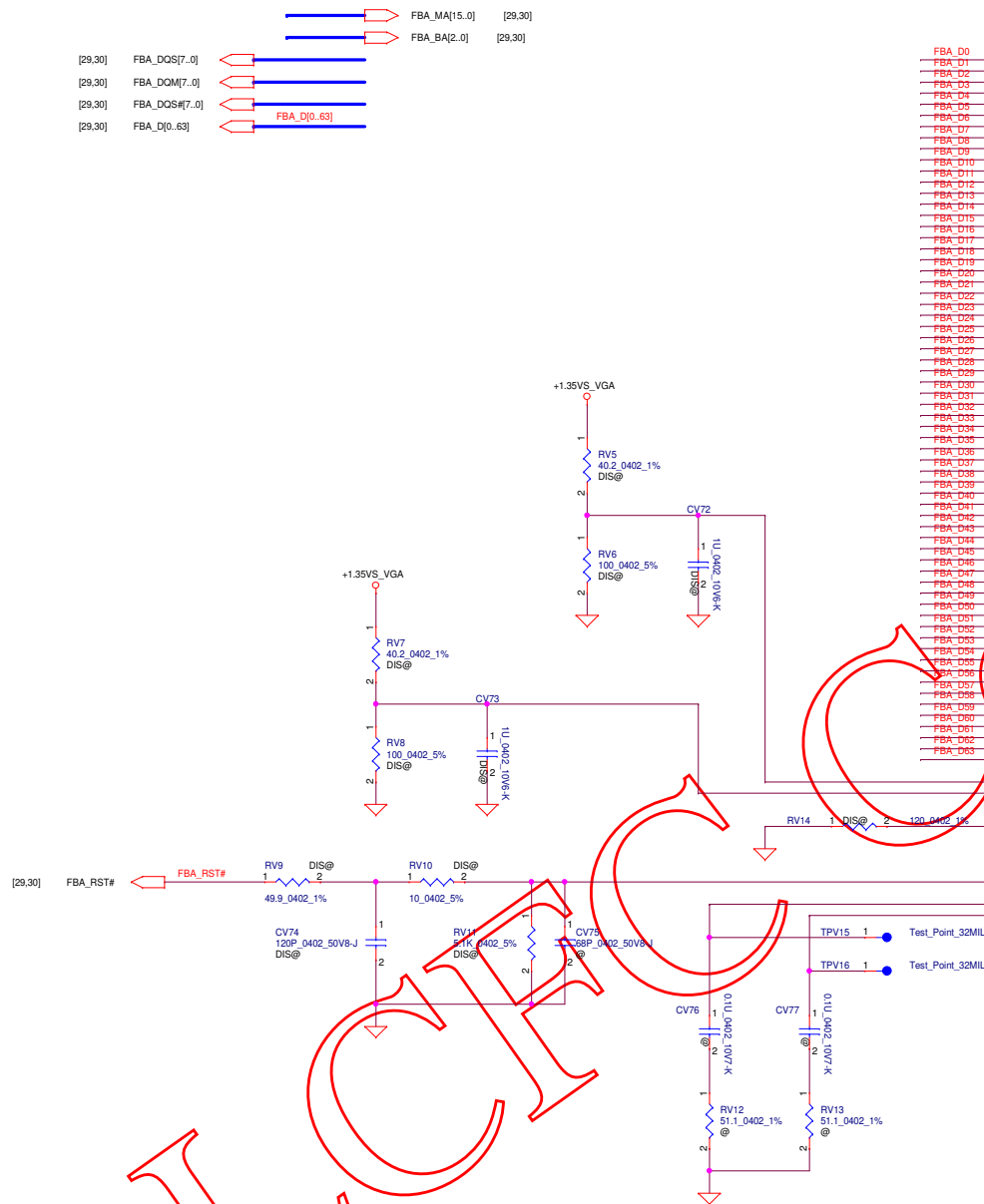
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Issued Date	2013/09/07	Deciphered Date	2014/09/07	Topaz & Jet Core Power	
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ASIC Ball	Topaz	Jet
U10, T10 AB13, W9 AB11, AB12 AC11, AC13 AC14, Y9, W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

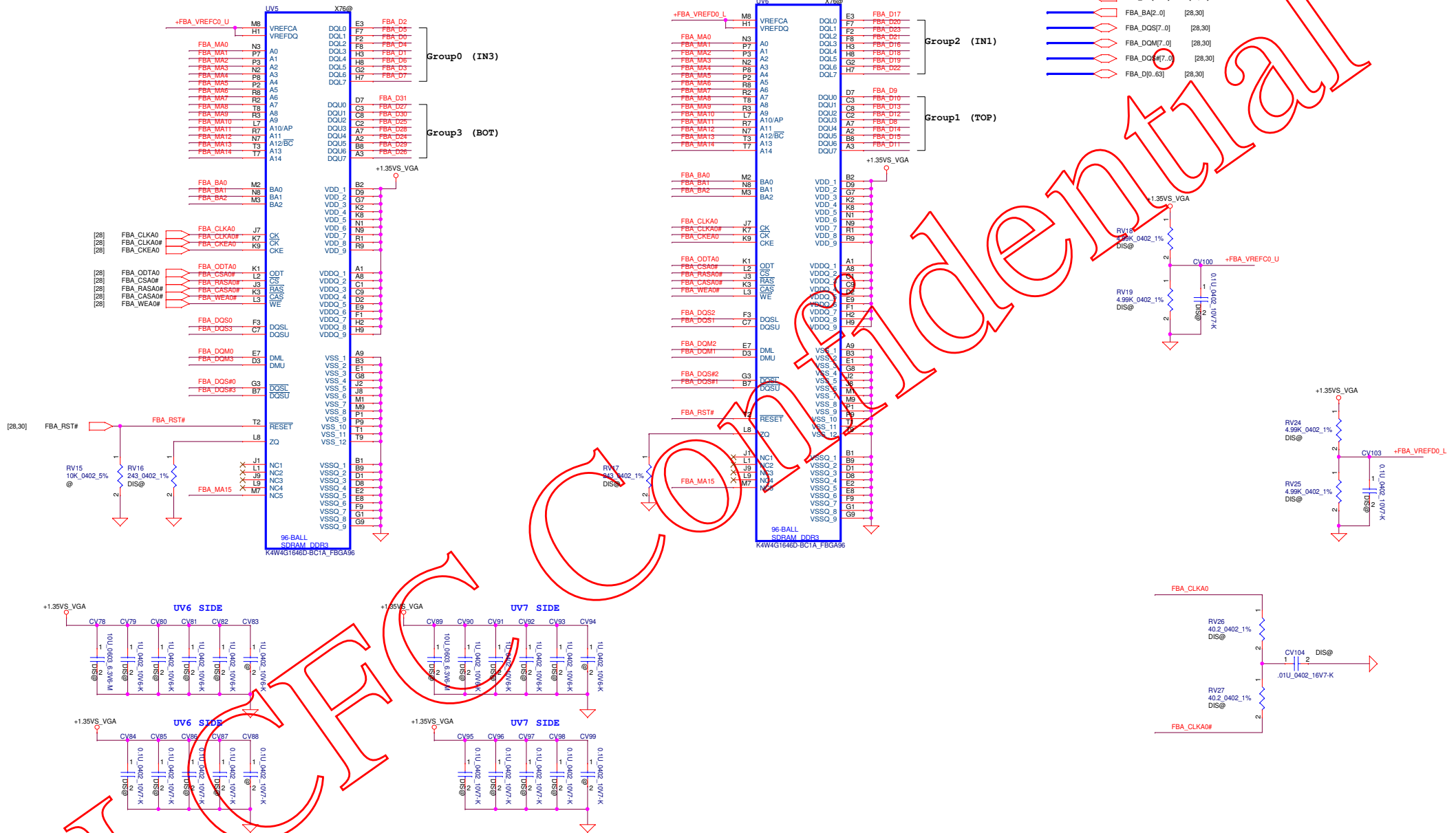
ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13, H16, H19, K10 J23, L24, M9, K10 K23, K24, K9, L11 L12, L13, L20, L21 L22	VDDMIO	VDDR1
AA17, AA18 AB17, AB18	VDD_GPIO33	VDDR3
AA20, AA21 AB20, AB21	VDD_GPIO18	VDD_CT


	Bits5	Bits4	Bits3	Bits2	Bits1
PS0	1	1	0	0	1
PS1	1	1	0	0	0
PS2	0	0	0	0	0
PS3	1	1	?	?	?

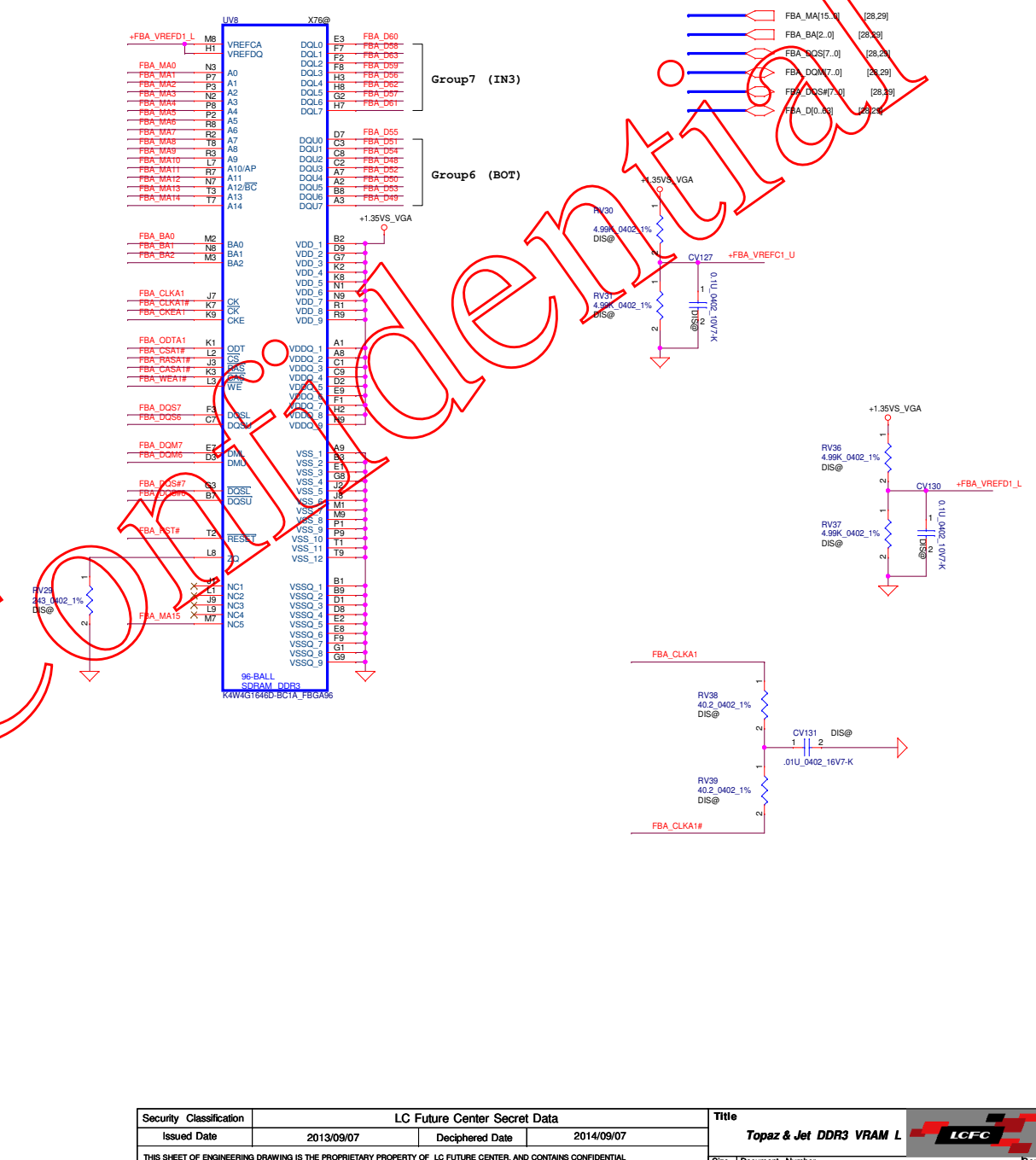


GDDR5/GDDR3		GDDR5/GDDR3		GDDR5/GDDR3	
FBA_D0	K27	DQA0_0	MAA0_0	K17	FBA_MA0
FBA_D1	H30	DQA0_1	MAA0_1	J20	FBA_MA1
FBA_D2	H30	DQA0_2	MAA0_2	H23	FBA_MA2
FBA_D3	H32	DQA0_3	MAA0_3	G23	FBA_MA3
FBA_D4	G29	DQA0_4	MAA0_4	H24	FBA_MA4
FBA_D5	F32	DQA0_5	MAA0_5	J19	FBA_MA5
FBA_D6	F32	DQA0_6	MAA0_6	K19	FBA_MA6
FBA_D7	F30	DQA0_7	MAA0_7	G20	FBA_MA7
FBA_D8	C30	DQA0_8	MAA0_8	L17	FBA_MA8
FBA_D9	F27	DQA0_9	MAA0_9	J14	FBA_MA9
FBA_D10	A28	DQA0_10	MAA1_0	K14	FBA_MA10
FBA_D11	C28	DQA0_11	MAA1_1	J11	FBA_MA11
FBA_D12	E27	DQA0_12	MAA1_2	J13	FBA_MA12
FBA_D13	G26	DQA0_13	MAA1_3	H11	FBA_MA13
FBA_D14	D28	DQA0_14	MAA1_4	G11	FBA_MA14
FBA_D15	F28	DQA0_15	MAA1_5	J16	FBA_MA15
FBA_D16	A25	DQA0_16	MAA1_6	L15	FBA_MA16
FBA_D17	C25	DQA0_17	MAA1_7	G14	FBA_MA17
FBA_D18	E25	DQA0_18	MAA1_8	L16	FBA_MA18
FBA_D19	D24	DQA0_19	MAA1_9	K1	FBA_MA19
FBA_D20	E23	DQA0_20	MAA1_0	E32	FBA_DQM0
FBA_D21	F23	DQA0_21	MAA1_1	E30	FBA_DQM1
FBA_D22	D22	DQA0_22	MAA1_2	A21	FBA_DQM2
FBA_D23	F21	DQA0_23	MAA1_3	C21	FBA_DQM3
FBA_D24	E21	DQA0_24	MAA1_4	E13	FBA_DQM4
FBA_D25	D20	DQA0_25	MAA1_5	D12	FBA_DQM5
FBA_D26	F19	DQA0_26	MAA1_6	E3	FBA_DQM6
FBA_D27	A19	DQA0_27	MAA1_7	F2	FBA_DQM7
FBA_D28	D18	DQA0_28	MAA1_8	E3	FBA_DQM8
FBA_D29	F17	DQA0_29	MAA1_9	E3	FBA_DQM9
FBA_D30	A17	DQA0_30	MAA1_0	E3	FBA_DQM10
FBA_D31	C17	DQA0_31	MAA1_1	E3	FBA_DQM11
FBA_D32	E17	DQA0_32	MAA1_2	E3	FBA_DQM12
FBA_D33	D16	DQA0_33	MAA1_3	E3	FBA_DQM13
FBA_D34	F15	DQA0_34	MAA1_4	E3	FBA_DQM14
FBA_D35	A15	DQA0_35	MAA1_5	E3	FBA_DQM15
FBA_D36	D14	DQA0_36	MAA1_6	E3	FBA_DQM16
FBA_D37	F13	DQA0_37	MAA1_7	E3	FBA_DQM17
FBA_D38	A13	DQA0_38	MAA1_8	E3	FBA_DQM18
FBA_D39	C13	DQA0_39	MAA1_9	E3	FBA_DQM19
FBA_D40	E11	DQA0_40	MAA1_0	E3	FBA_DQM20
FBA_D41	A11	DQA0_41	MAA1_1	E3	FBA_DQM21
FBA_D42	C11	DQA0_42	MAA1_2	E3	FBA_DQM22
FBA_D43	F11	DQA0_43	MAA1_3	E3	FBA_DQM23
FBA_D44	A9	DQA0_44	MAA1_4	E3	FBA_DQM24
FBA_D45	C9	DQA0_45	MAA1_5	E3	FBA_DQM25
FBA_D46	F9	DQA0_46	MAA1_6	E3	FBA_DQM26
FBA_D47	D8	DQA0_47	MAA1_7	E3	FBA_DQM27
FBA_D48	E7	DQA0_48	MAA1_8	E3	FBA_DQM28
FBA_D49	A7	DQA0_49	MAA1_9	E3	FBA_DQM29
FBA_D50	C7	DQA0_50	MAA1_0	E3	FBA_DQM30
FBA_D51	E7	DQA0_51	MAA1_1	E3	FBA_DQM31
FBA_D52	F7	DQA0_52	MAA1_2	E3	FBA_DQM32
FBA_D53	A5	DQA0_53	MAA1_3	E3	FBA_DQM33
FBA_D54	C5	DQA0_54	MAA1_4	E3	FBA_DQM34
FBA_D55	F5	DQA0_55	MAA1_5	E3	FBA_DQM35
FBA_D56	D5	DQA0_56	MAA1_6	E3	FBA_DQM36
FBA_D57	E5	DQA0_57	MAA1_7	E3	FBA_DQM37
FBA_D58	A5	DQA0_58	MAA1_8	E3	FBA_DQM38
FBA_D59	C5	DQA0_59	MAA1_9	E3	FBA_DQM39
FBA_D60	F5	DQA0_60	MAA1_0	E3	FBA_DQM40
FBA_D61	D5	DQA0_61	MAA1_1	E3	FBA_DQM41
FBA_D62	E5	DQA0_62	MAA1_2	E3	FBA_DQM42
FBA_D63	A5	DQA0_63	MAA1_3	E3	FBA_DQM43


Memory Partition A - Lower 32 bits




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				Date:	Wednesday, August 05, 2015	Sheet 29 of 83
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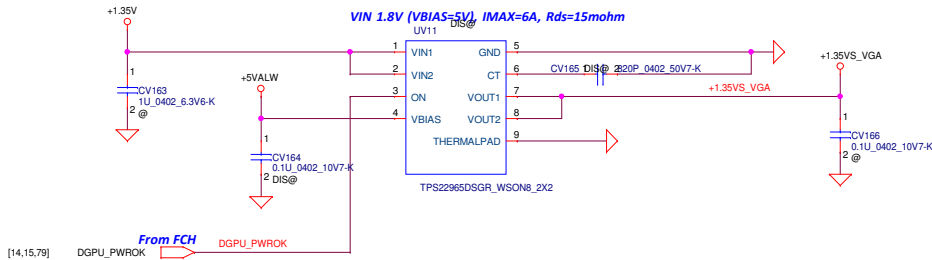
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				Date: Wednesday, August 05, 2015	Sheet 31 of 83	

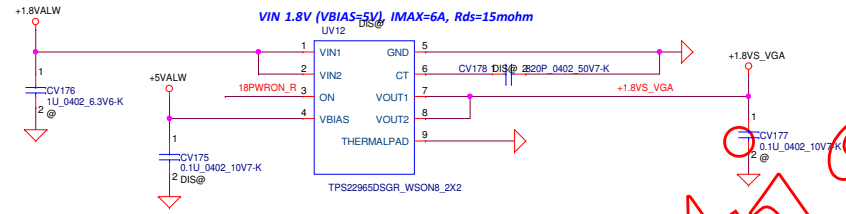
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				Date:	Wednesday, August 05, 2015	Sheet	32 of 83

+1.35V to +1.35VS_VGA

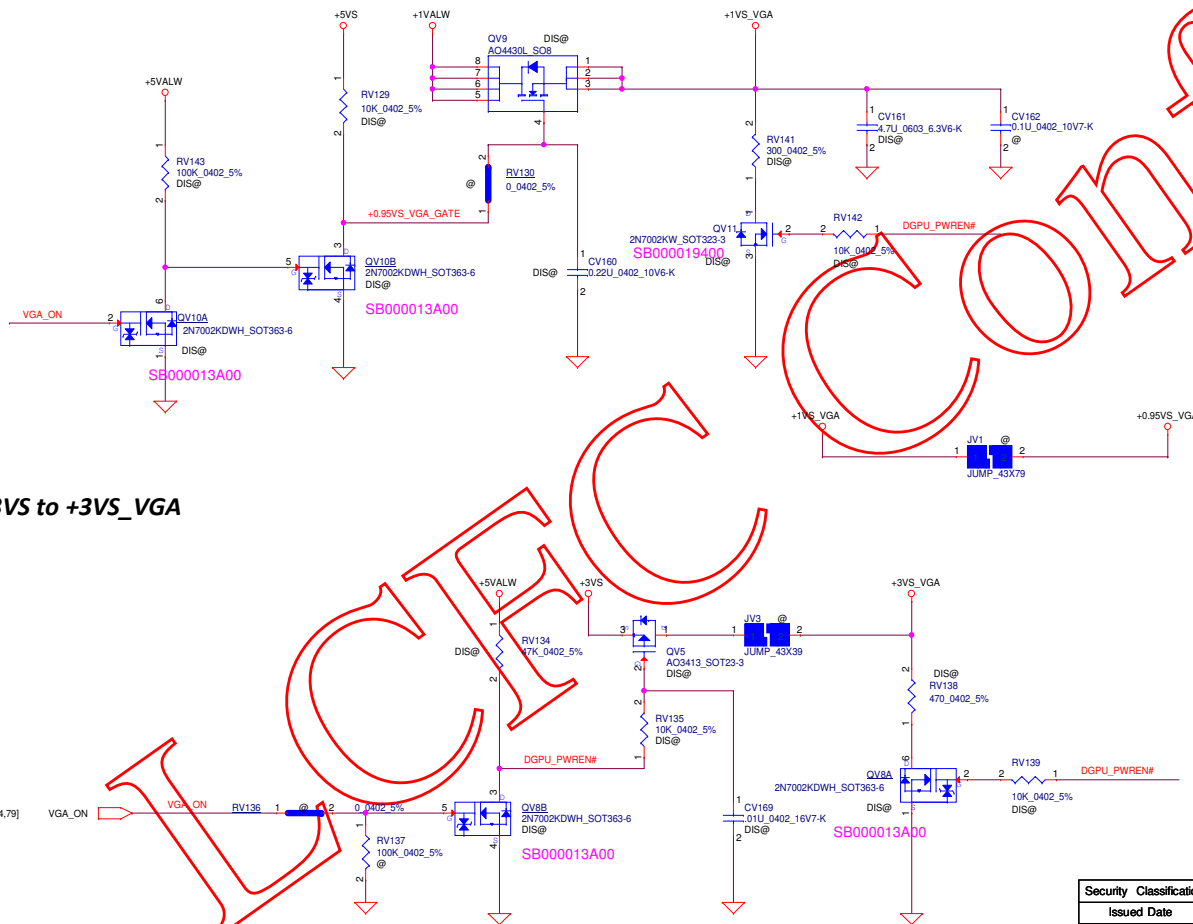


+1.8VALW to +1.8VS_VGA

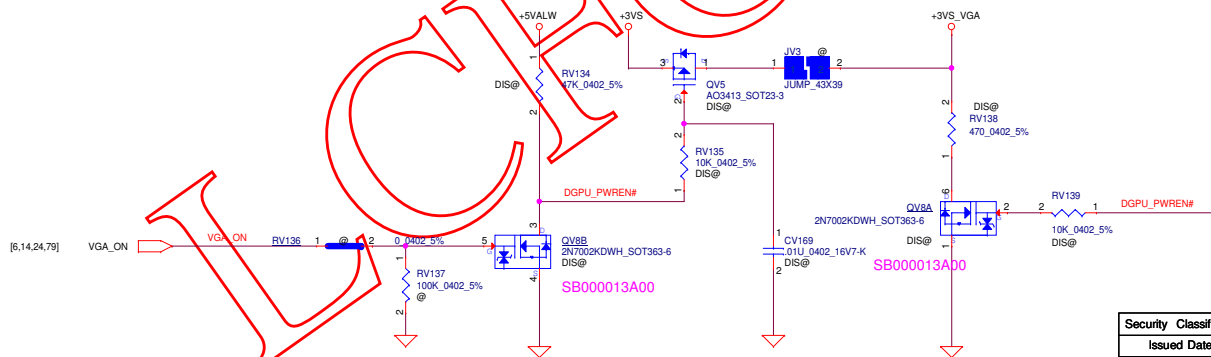


MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

+1VALW to +1VS_VGA




+3VS to +3VS_VGA




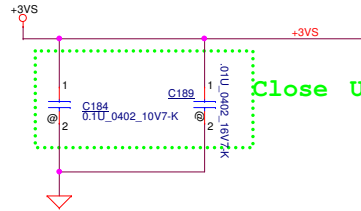
PS_0[1]	ROM_CONFIG[0]	STRAP BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[2]	ROM_CONFIG[1]	
PS_0[3]	ROM_CONFIG[2]	
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1]	BOARD_CONFIG[0]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[2]	BOARD_CONFIG[1]	
PS_3[3]	BOARD_CONFIG[2]	
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

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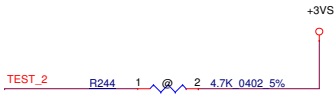
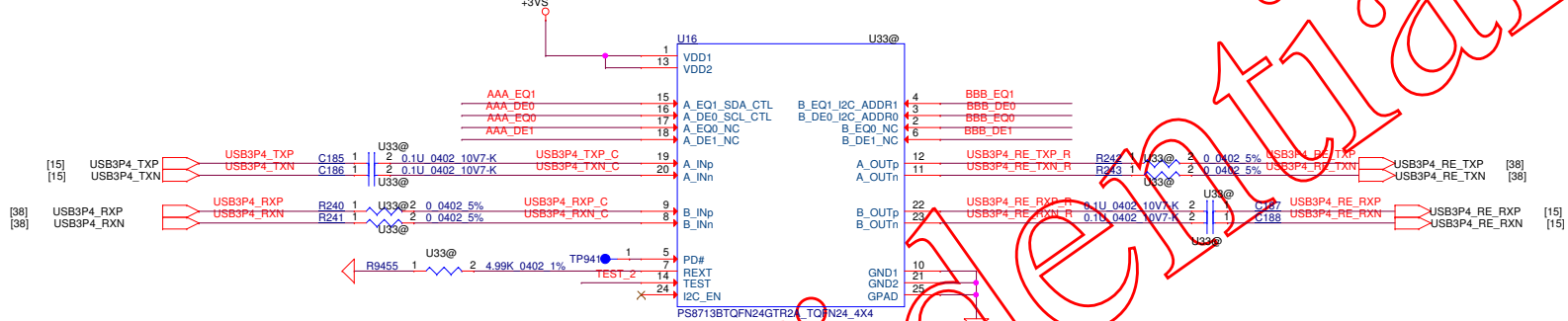
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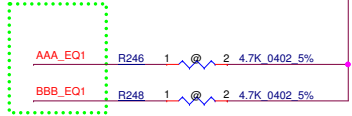
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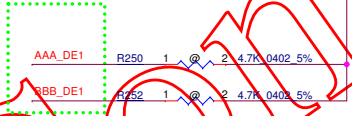
USB3.0 Repeater Port 3



Normal LFPS mode
Internal PD

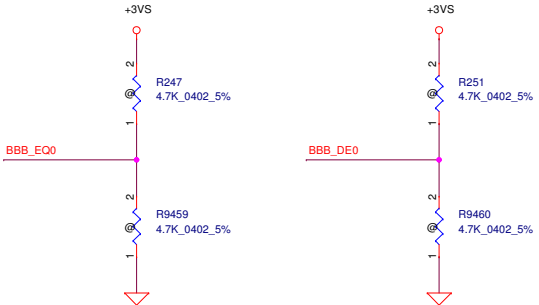
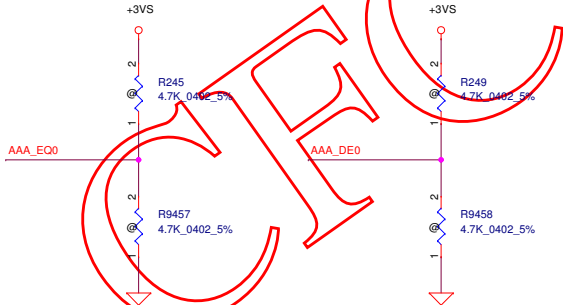
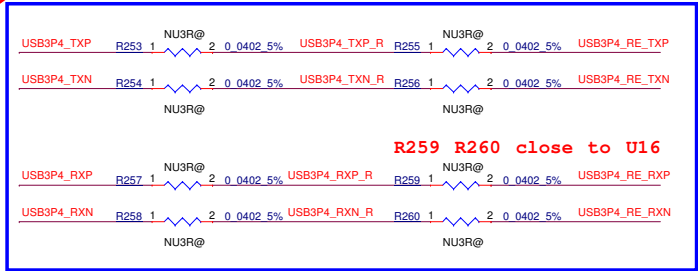


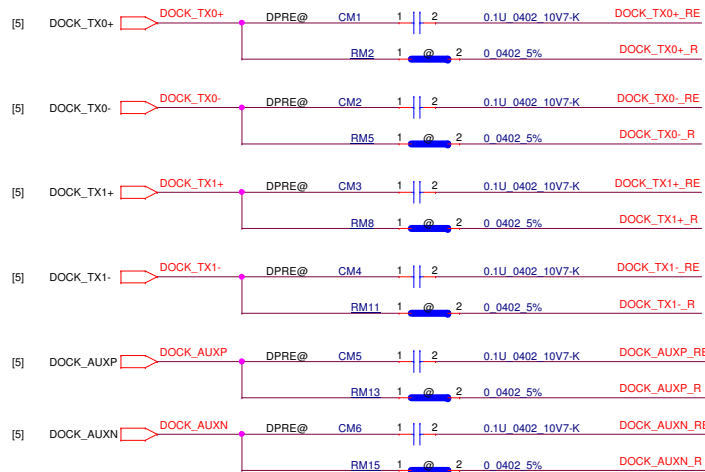
EQ Default 9.5dB
Internal PD



de-emphasis Default 3.5dB
Internal PD

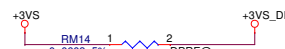
20-lay 0-ohm



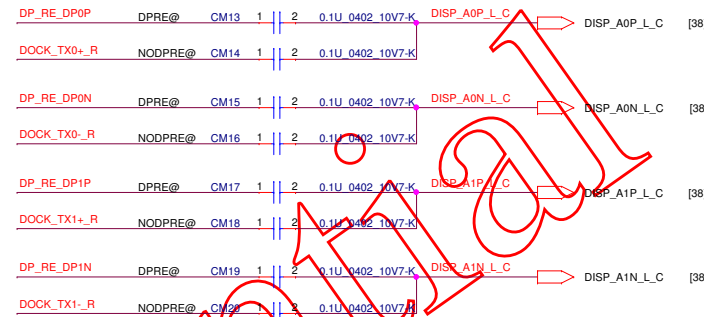
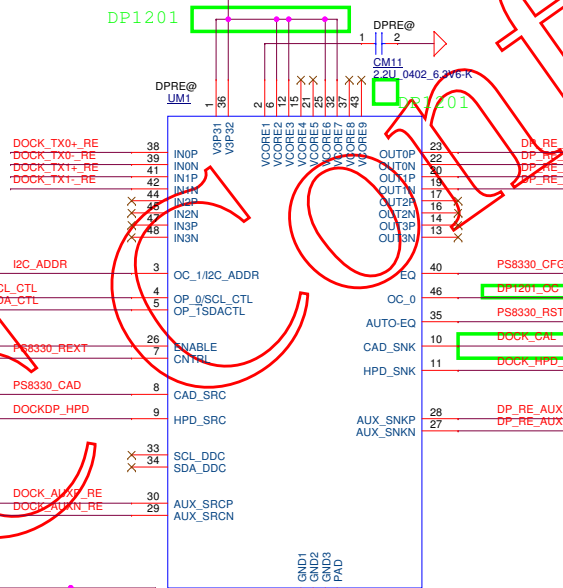


Cap.Pin1 and R.Pin1 Co-lay

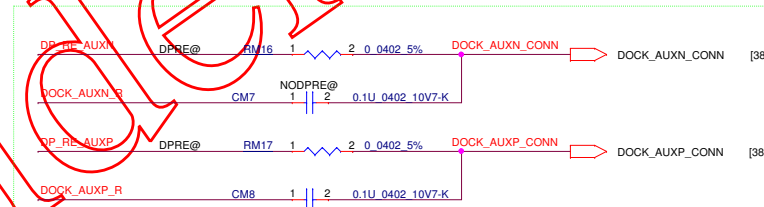
One-Link DP Repeater



DP1201

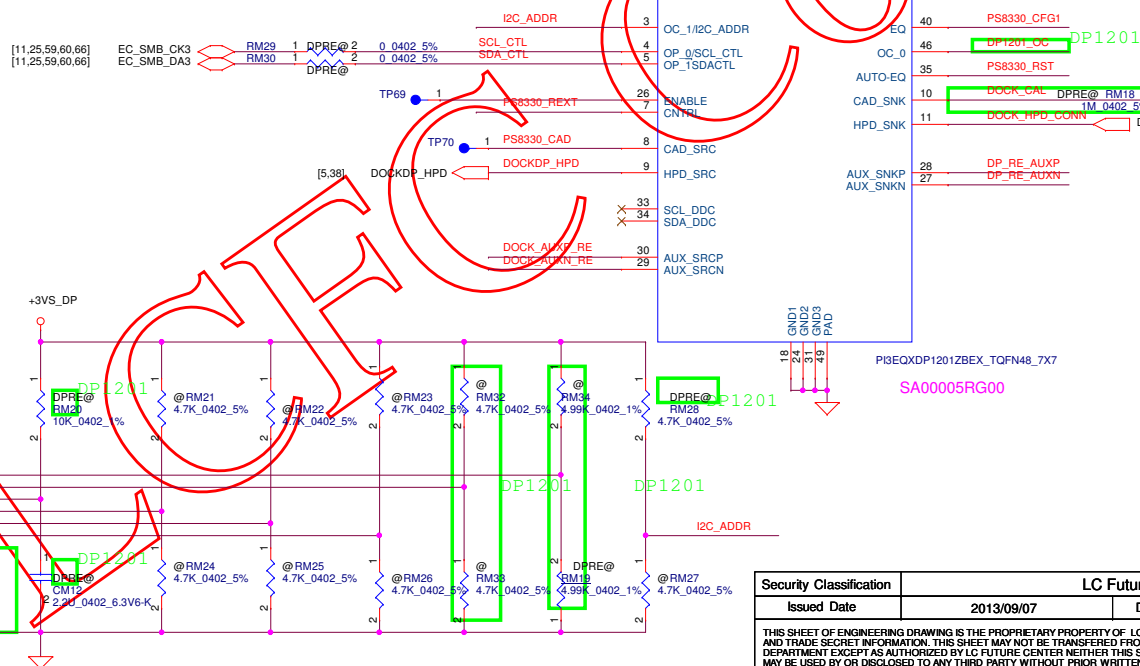


R.Pin2 and R.Pin2 Co-lay



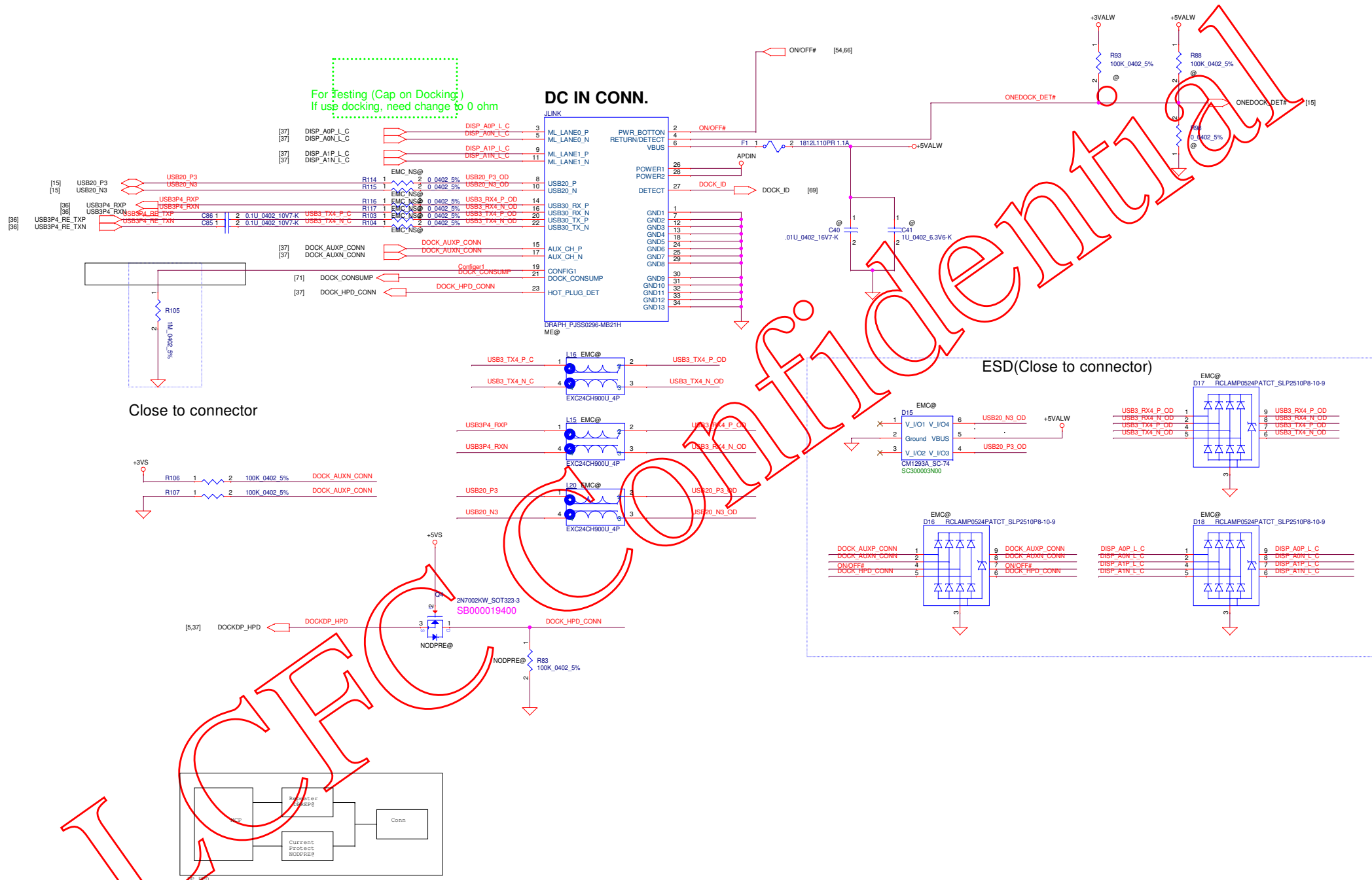
Cap.Pin2 and R.Pin2 Co-lay


DP AUX : From Repeater don't need cap, but PCH.

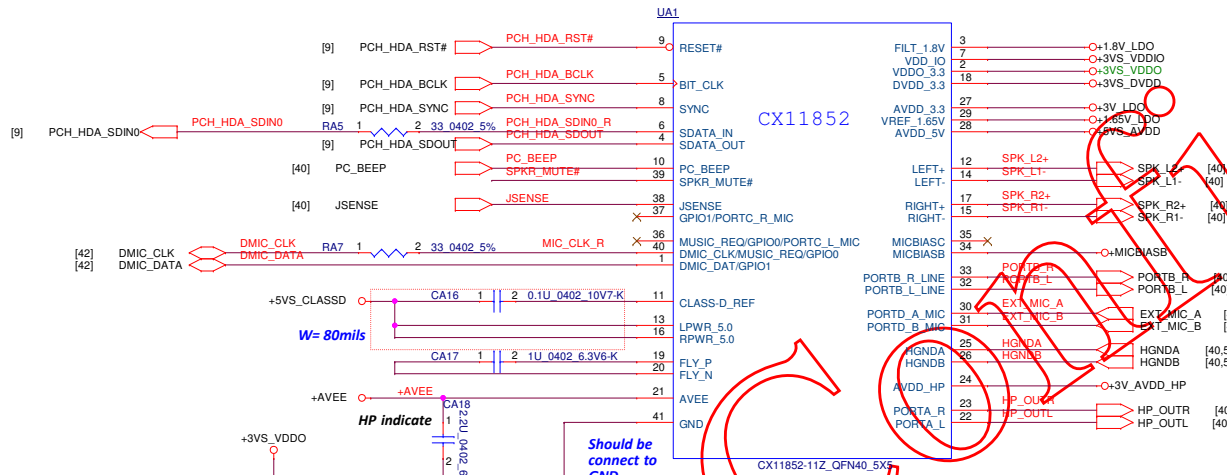
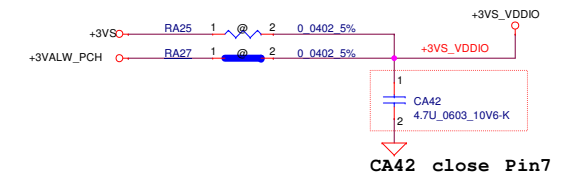
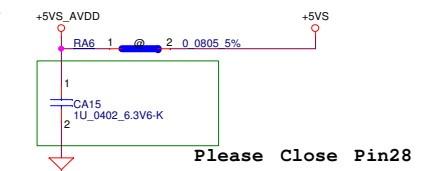
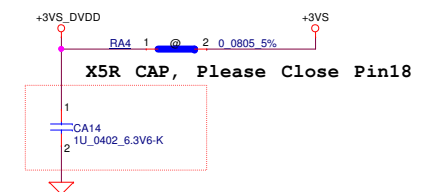
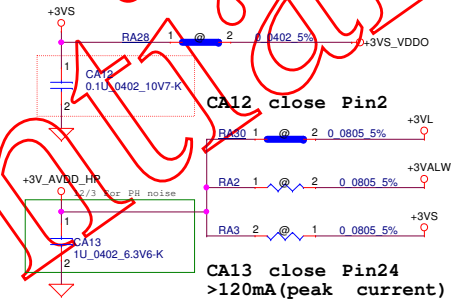
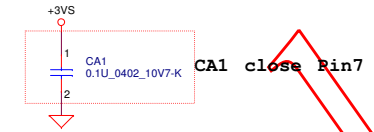
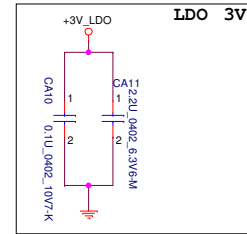
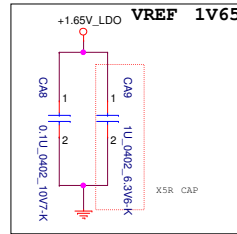
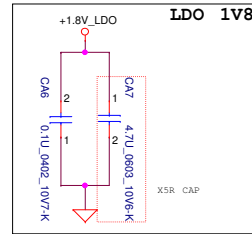
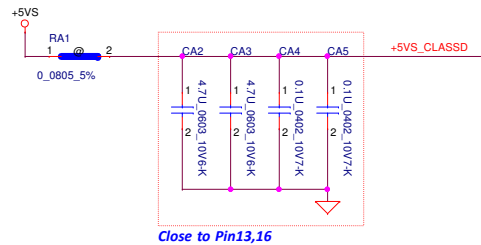


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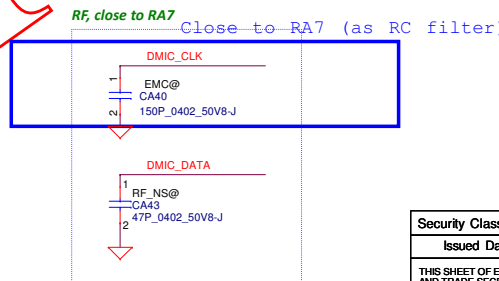
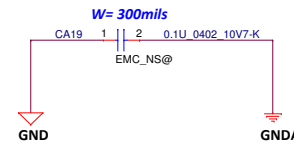
Title		
DP-DOCKING RP		
Size	Document Number	Rev
Custom	BE460 NM-A551	1.0
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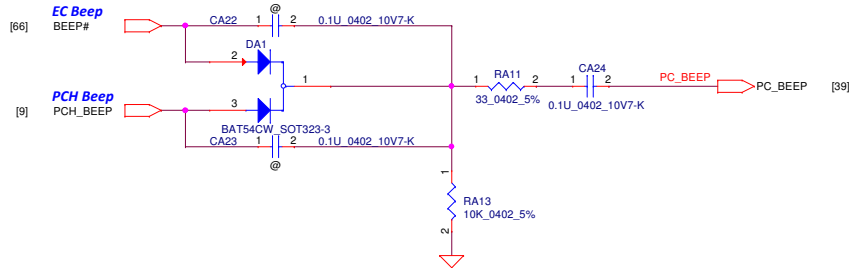
Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A
HGND A/HGND B trace widths should be as wide as possible



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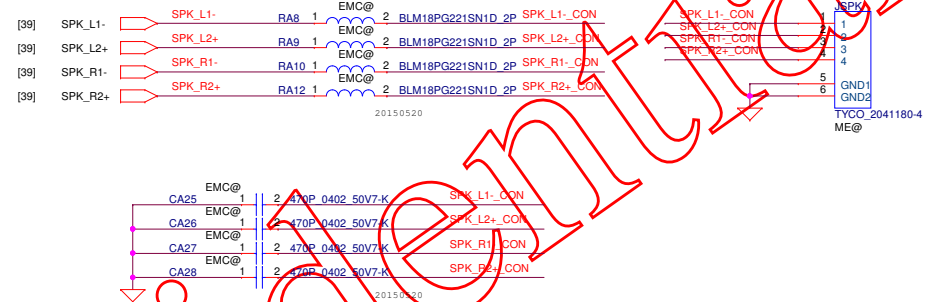
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CX11852 & SPEAKER		
Size	Document Number	Rev
Custom	BE460 NM-A551	1.0
Date:	Wednesday, August 05, 2015	Sheet 39 of 83

PC BEEP



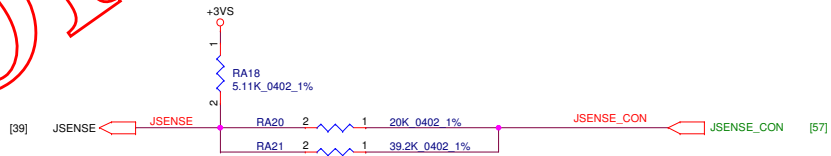
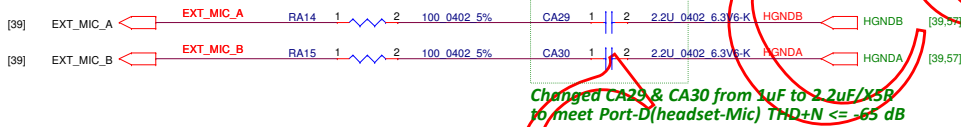
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SPK CONN.

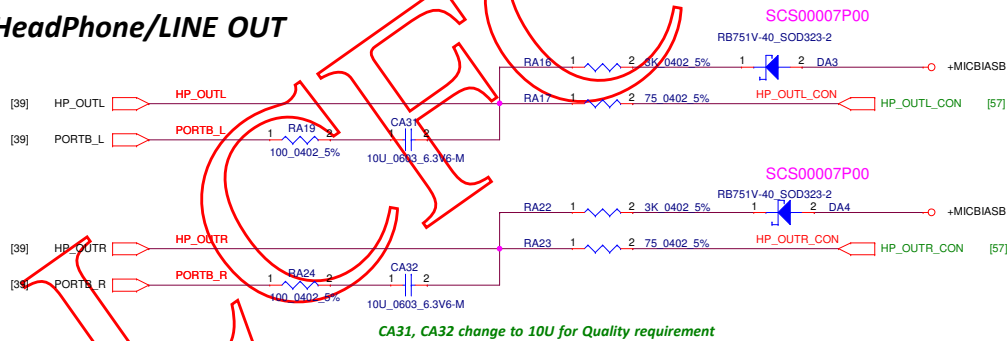



EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A



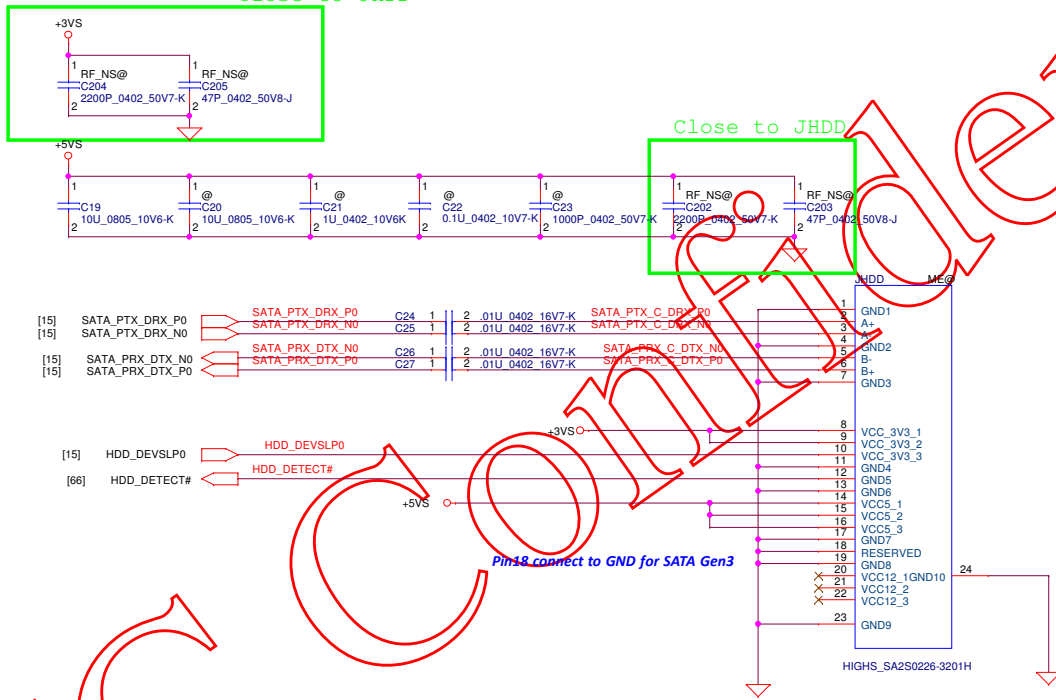
HeadPhone/LINE OUT



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Custom							
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A circuit diagram showing a 2200pF capacitor (C204) connected between two RF pins. The left pin is labeled 'RF_NS@' and the right pin is labeled 'RF_NS@'. The capacitor is represented by two parallel lines. The value '2200P_0402_50V7-K' is written below the capacitor. The pins are connected to a +3VS supply and a ground symbol.


Close to JHDD



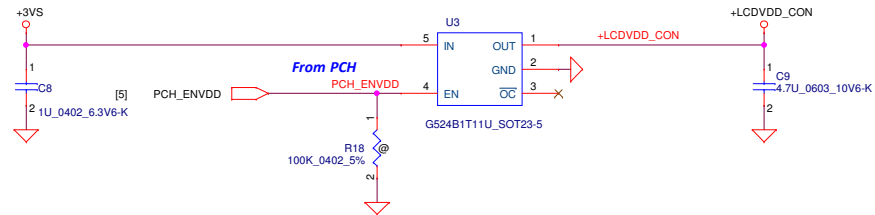
Pin18 connect to GND for SATA Gen3

HIGHS_SA2S0226-3201H

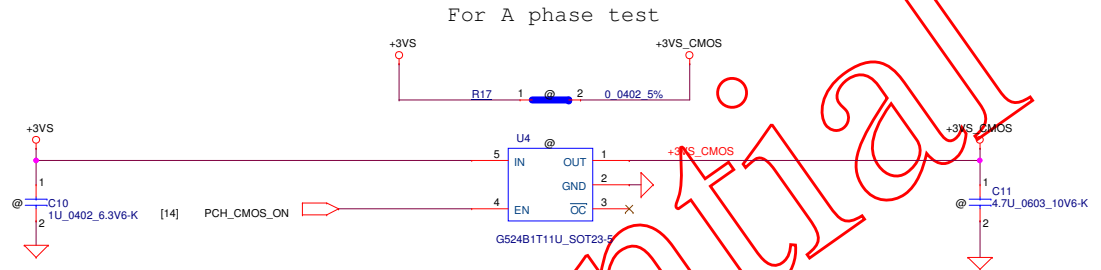
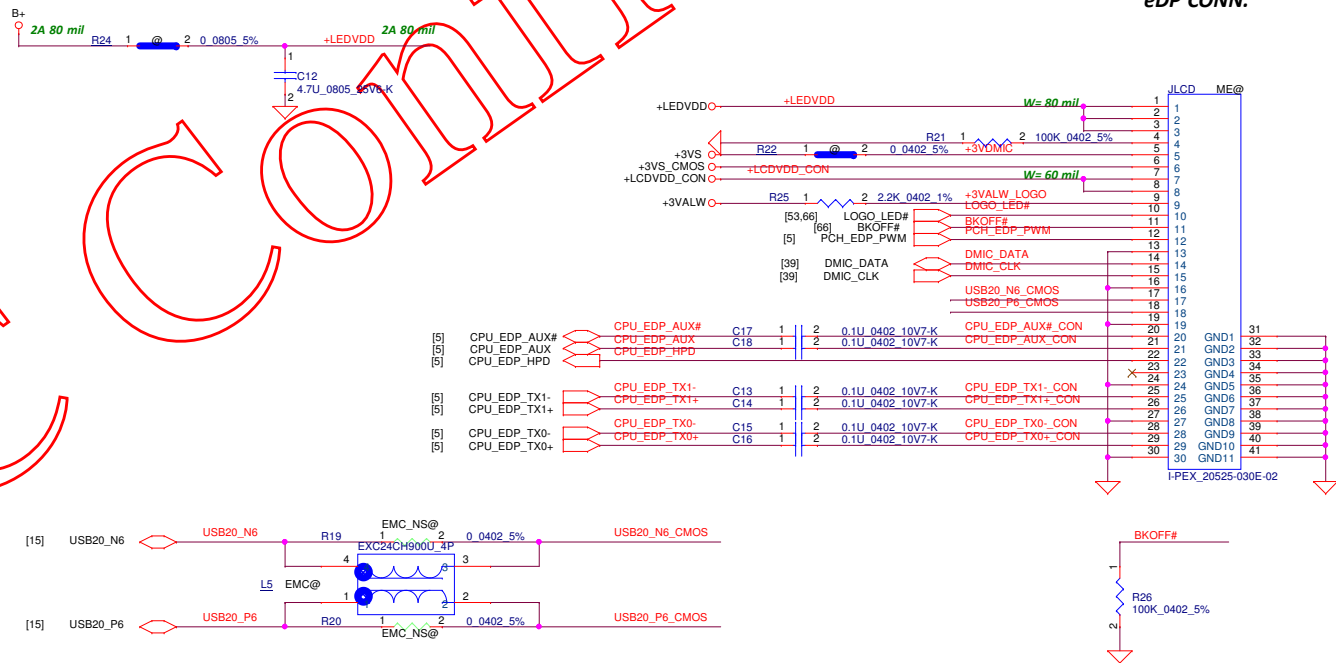
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Issued Date	2013/09/07	Deciphered Date	2014/09/07
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Title			
SATA HDD/ODD			
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Date:	Wednesday, August 05, 2015	Sheet	41 of 83

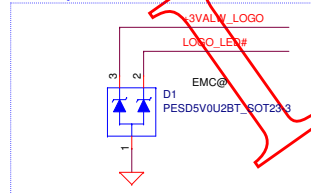
LCDVDD Circuit



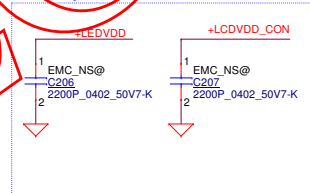
CMOS Camera


**eDP CONN.**

ESD request

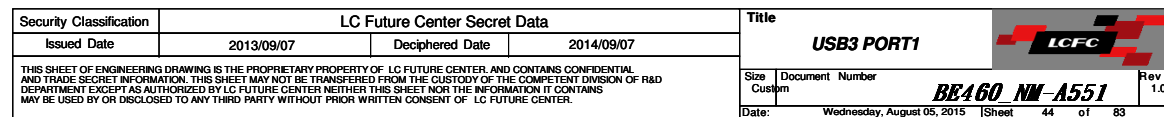


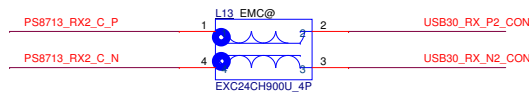
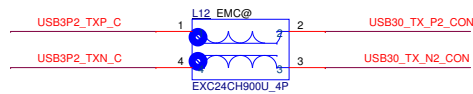
~~EMC request , Close to JLCD~~



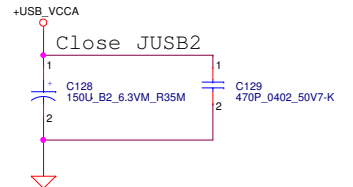
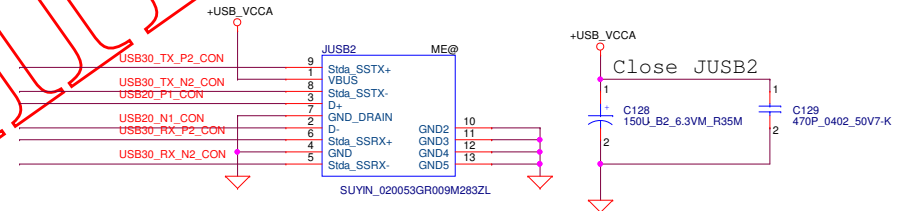
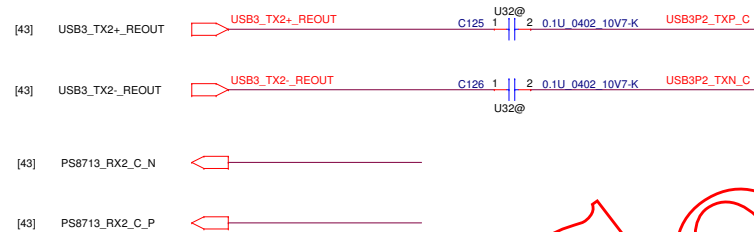
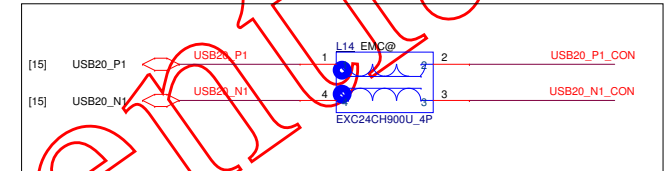
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Issued Date	2013/09/07	Deciphered Date	2014/09/07	eDP/CMOS		
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				Date: Wednesday, August 05, 2015		Sheet 42 of 83

For 14" use(14" on board USB don't support S&C
,But 15" on board USB support S&C.S&C IC always on MB)

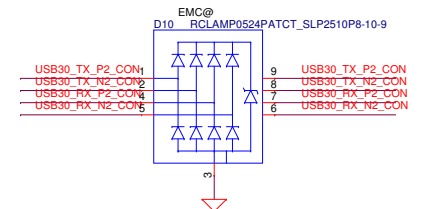
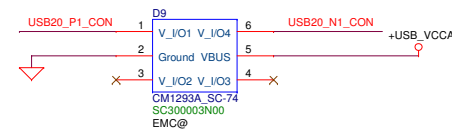
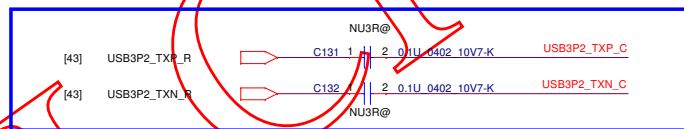





Co-layout L15 for EMI test




Co-lay 0-ohm




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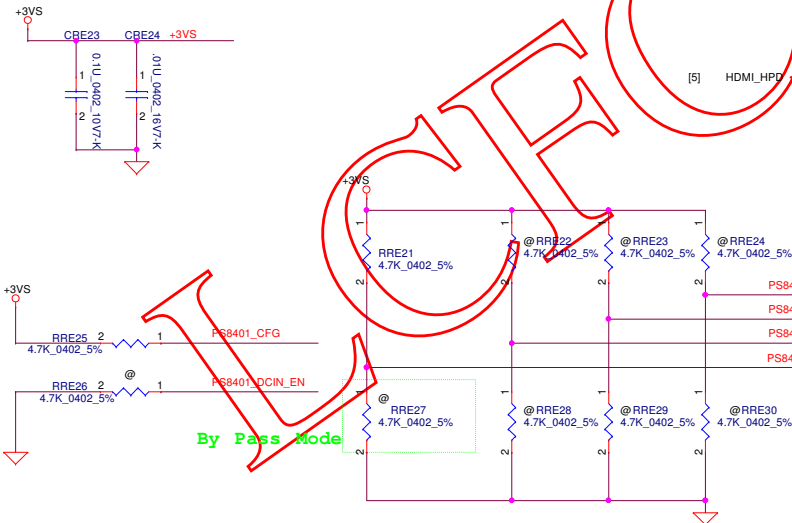
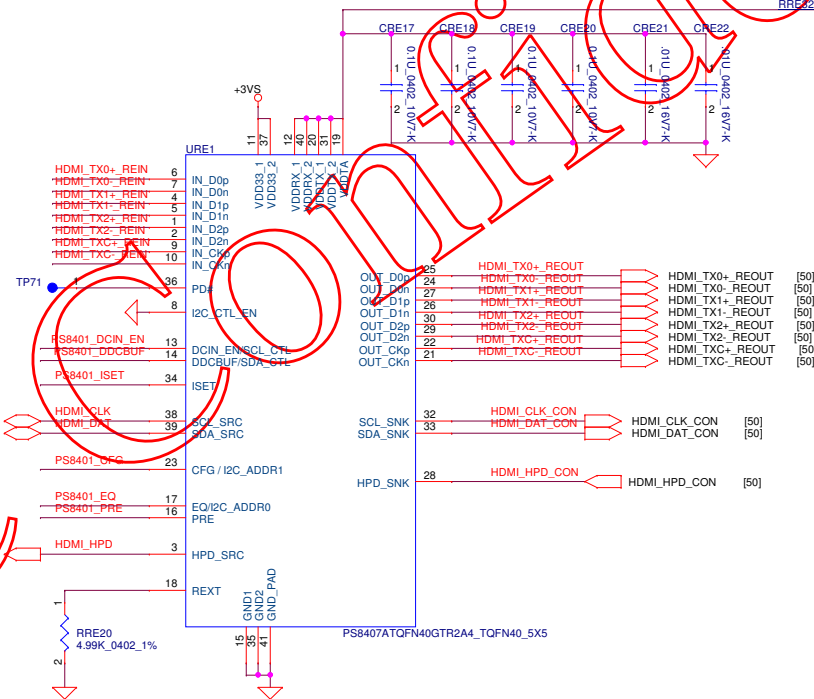
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				Date:	Wednesday, August 05, 2015	Rev 1.0
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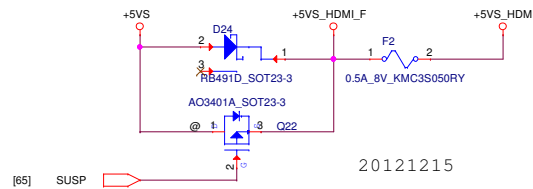
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HDMI Repeater

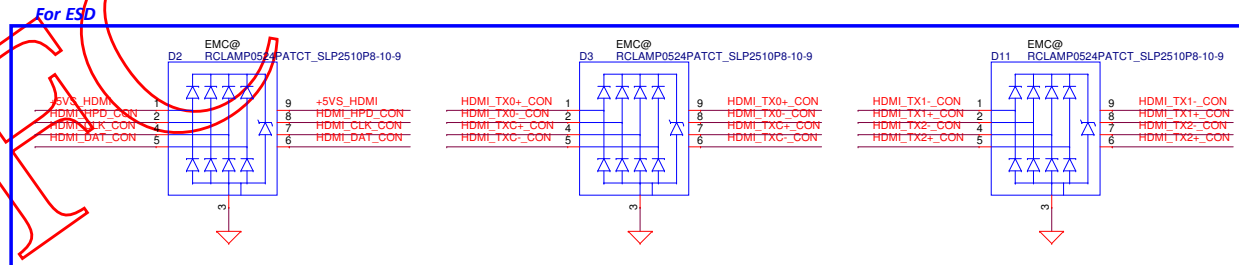
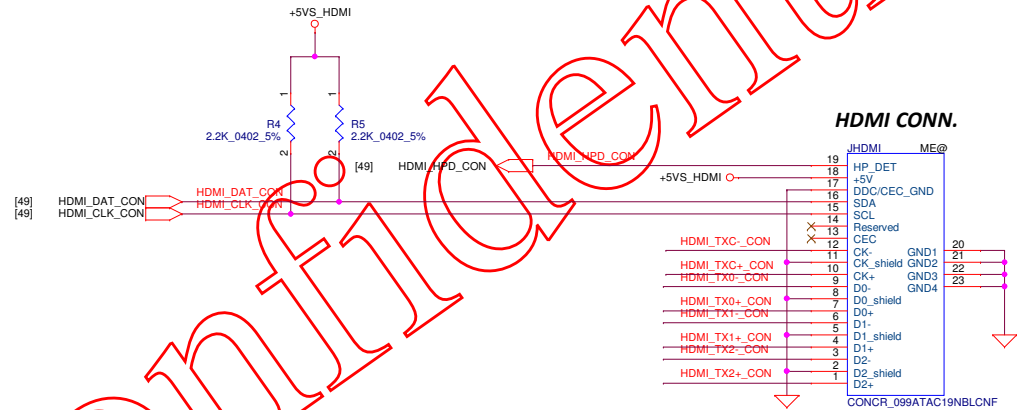
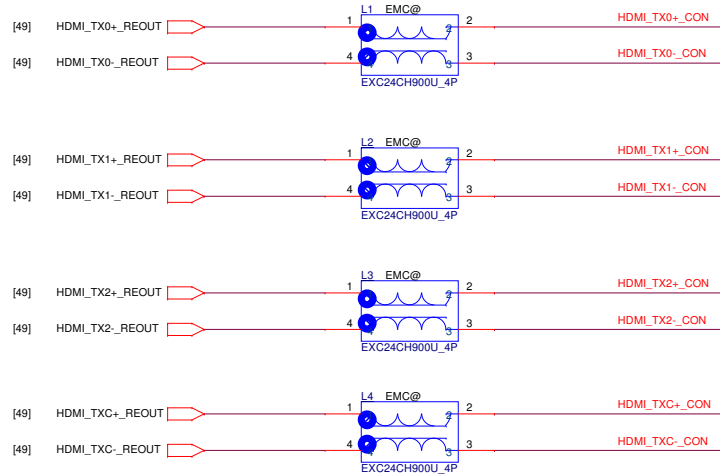


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Title			
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20121215

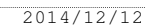
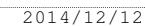
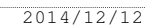
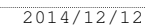


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2014/12/12

2014/12/12

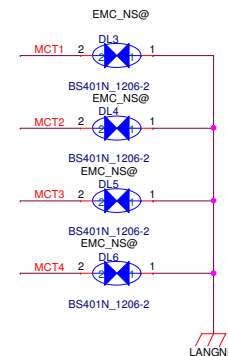
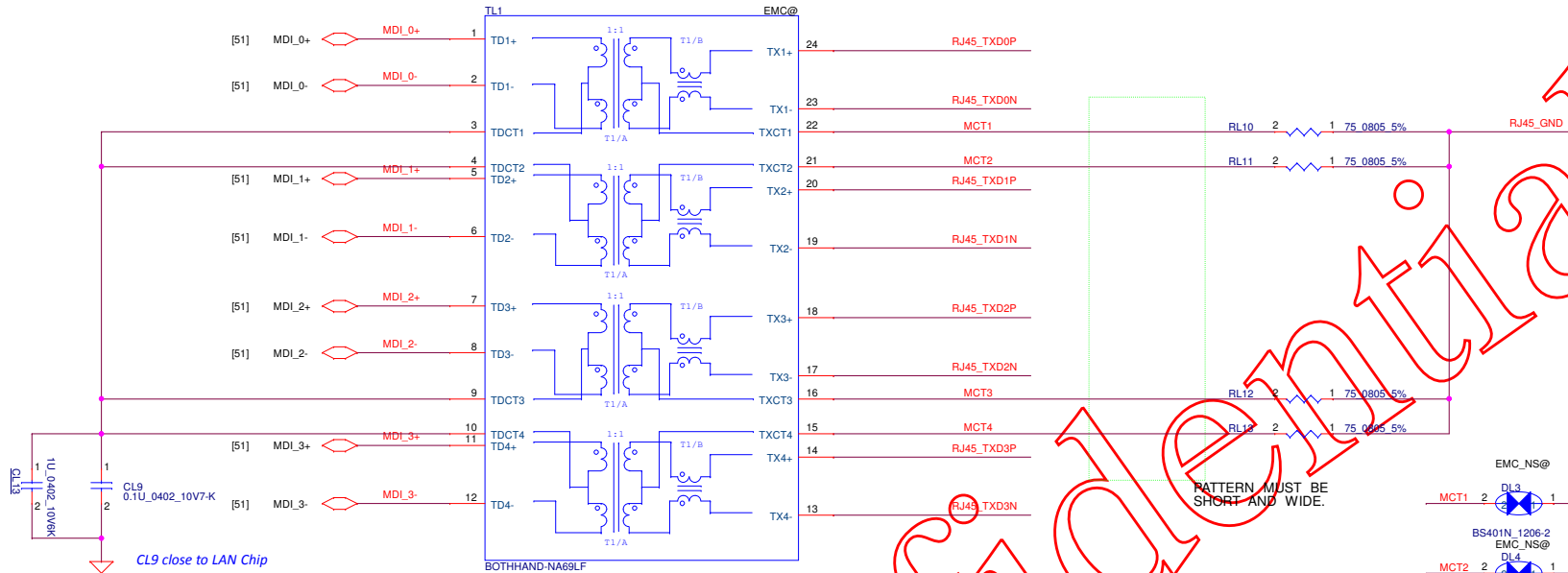


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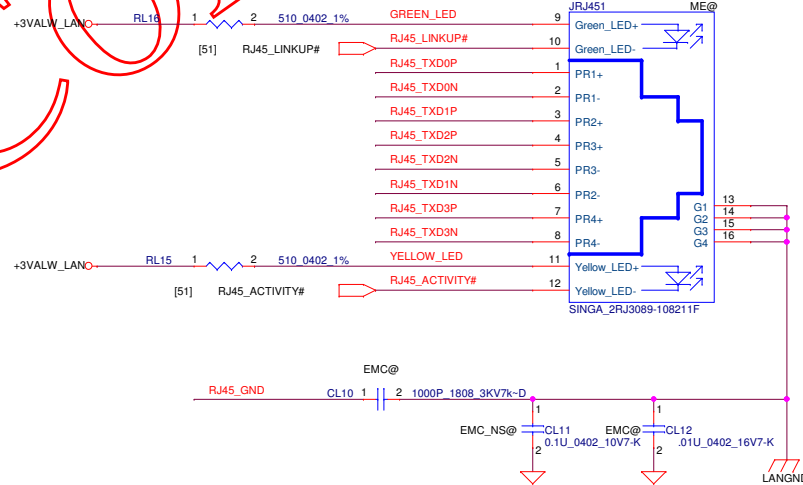
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2014/12/12



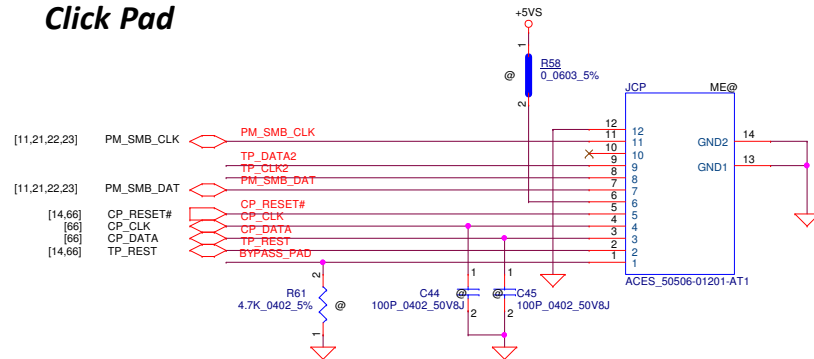
RJ-45 Conn.



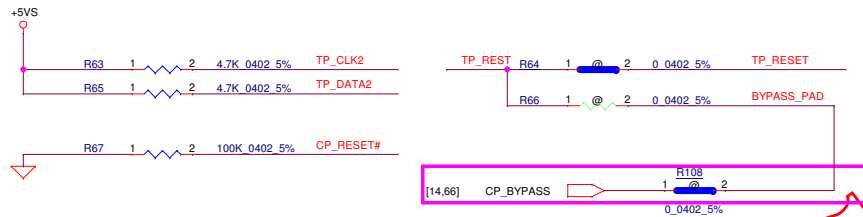
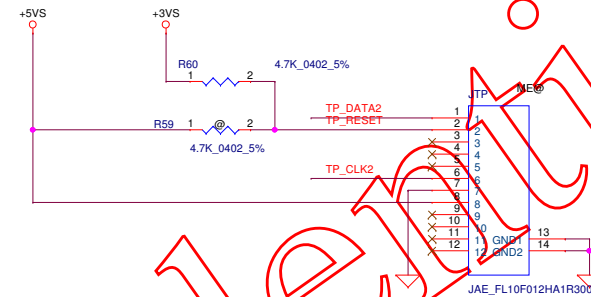
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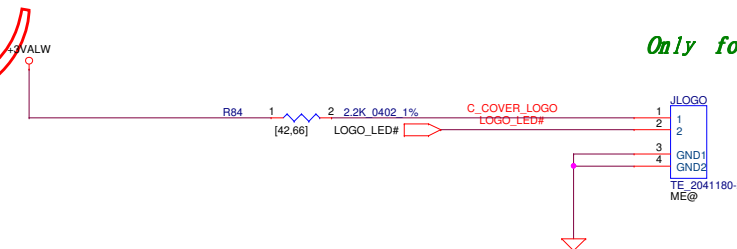
Click Pad



Track point

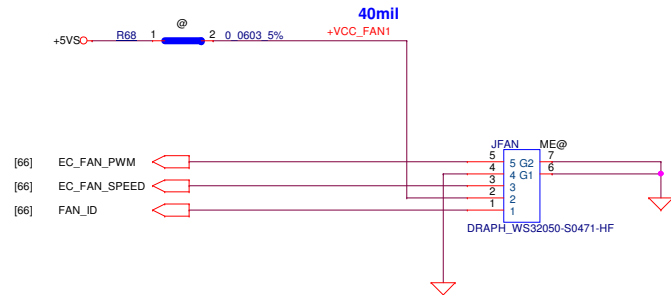


Only for Edge 14"



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				Date:	Wednesday, August 05, 2015		Sheet	53	of 83

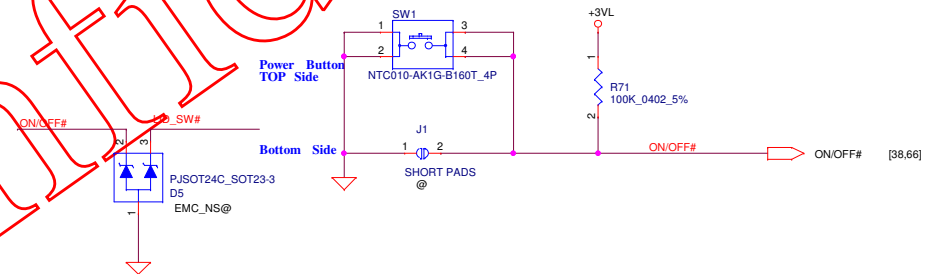
FAN CONN.



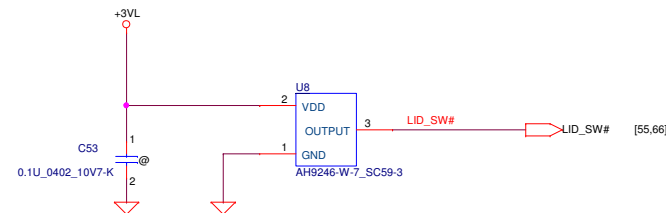
PWR BTN/LID SW CONN.

For 14" on board
For 15" on Sub/B

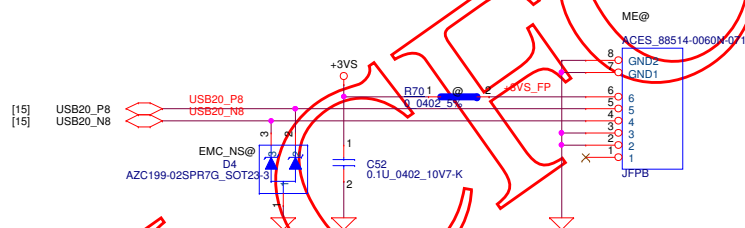
ON/OFF switch




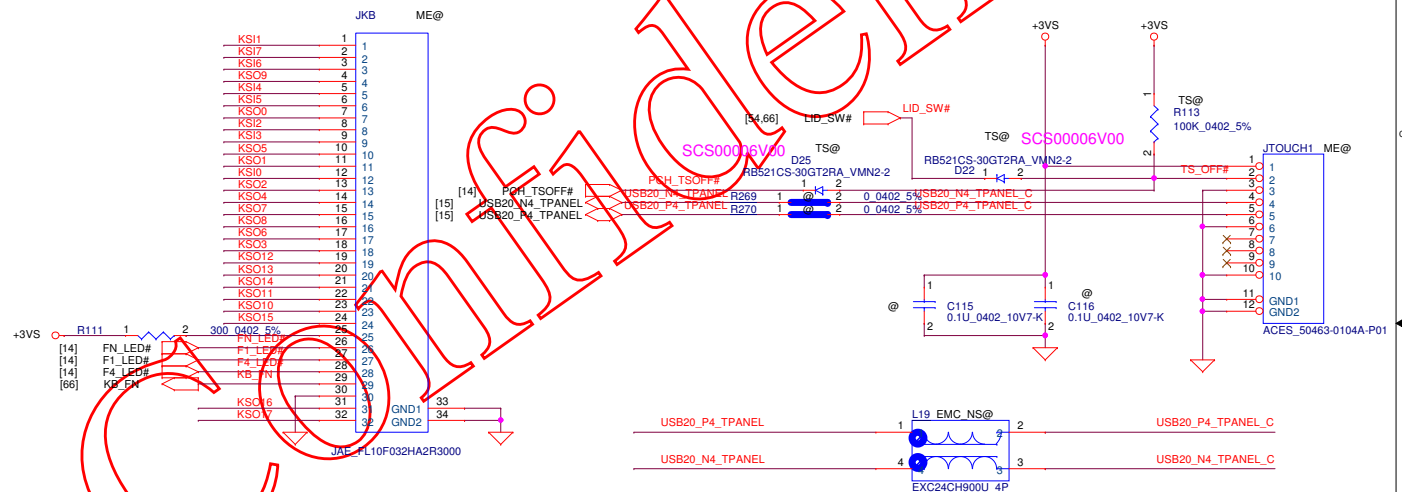
Lid Switch




FingerPrint CONN.



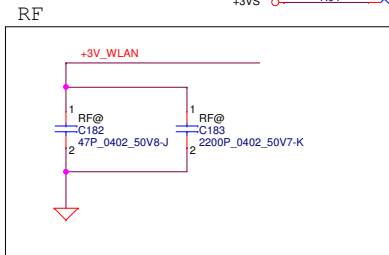
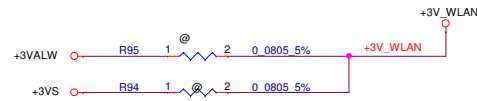
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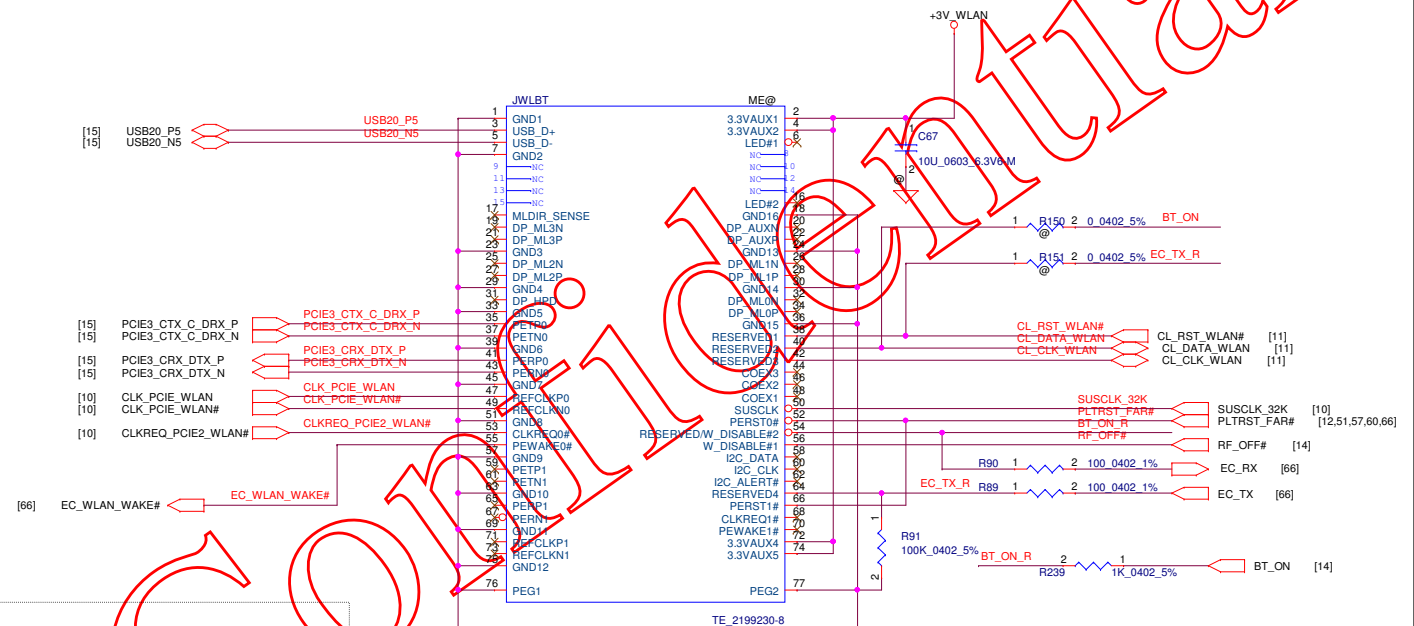
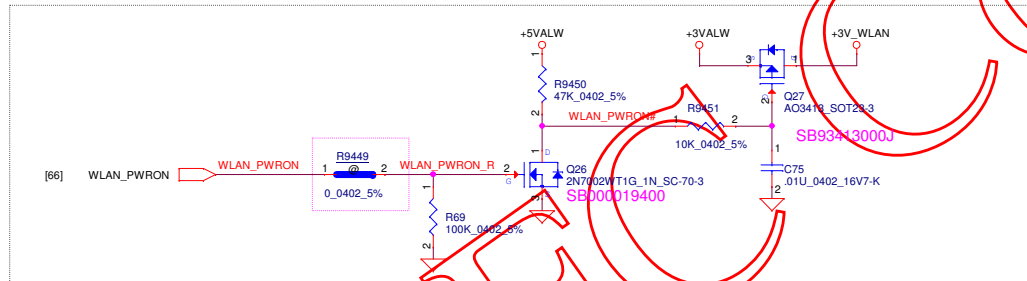
LCFEC

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				Document Number BE460 NW-A551		Rev 1.0
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3.2H CONNECTOR

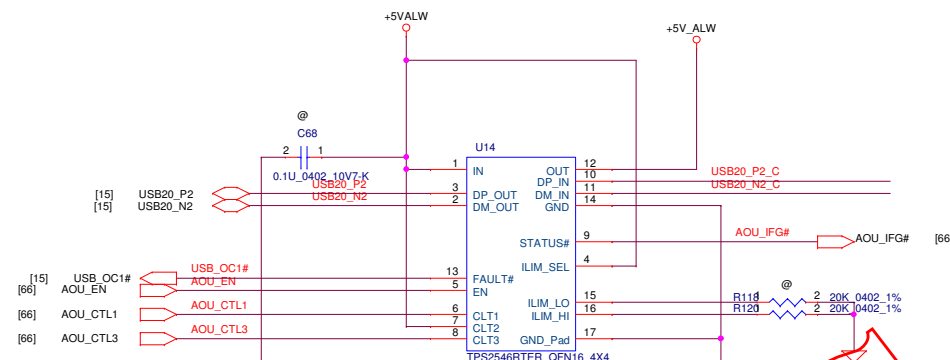


Close to Conn.



For 14"
CardReader Board - FFC

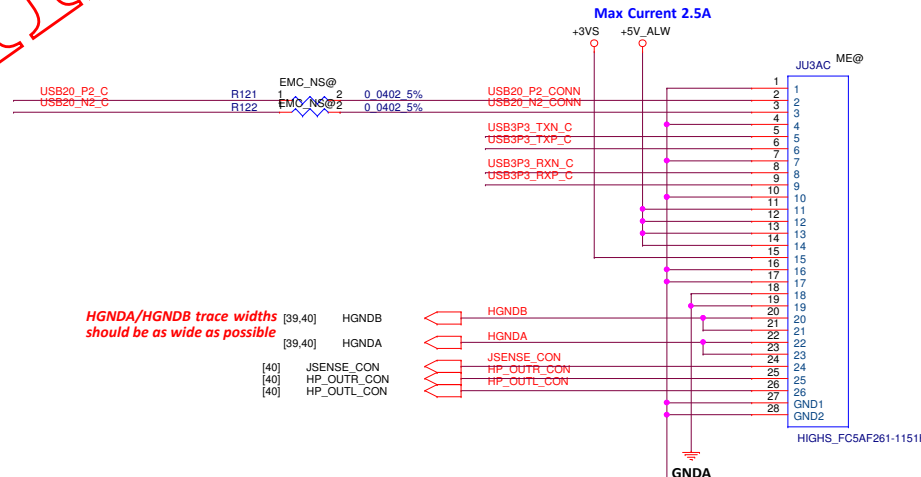
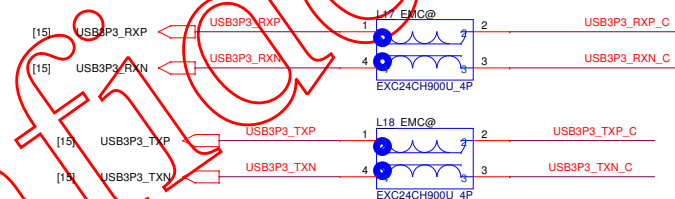
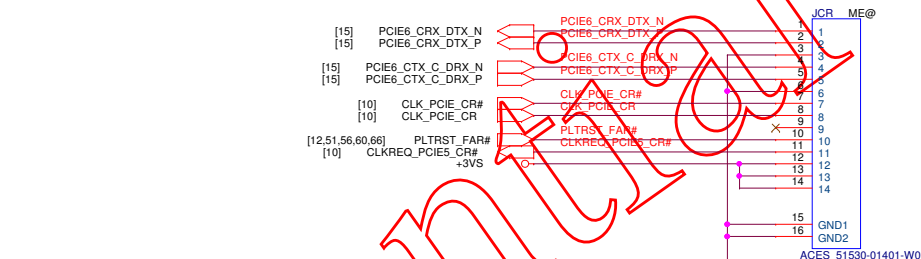
For 14" S&C IC on MB) S&C port on SUB/B



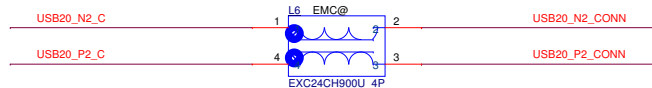
TI TPS2546

CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP Bc 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active



USB_OC5# to MCP
AOU_EN to EC
AOU_CTL1 to EC
AOU_CTL3 to EC
AOU_IFG# to EC



HGND A/HGND B trace widths should be as wide as possible

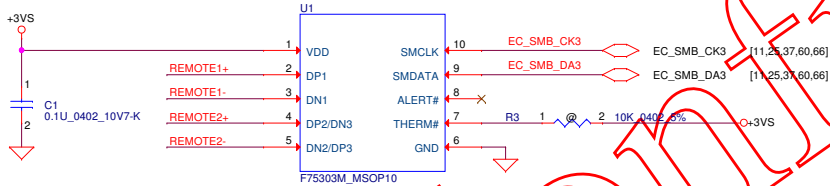


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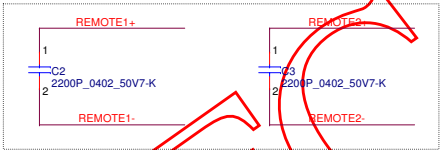
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Thermal Sensor

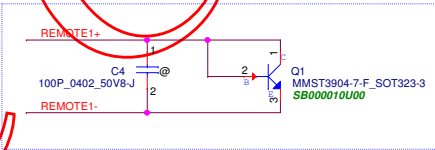
Thermal Sensor
placed near by VRAM



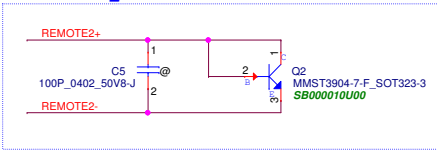
Close to U1



Under VRAM



Close to +VCC_CORE

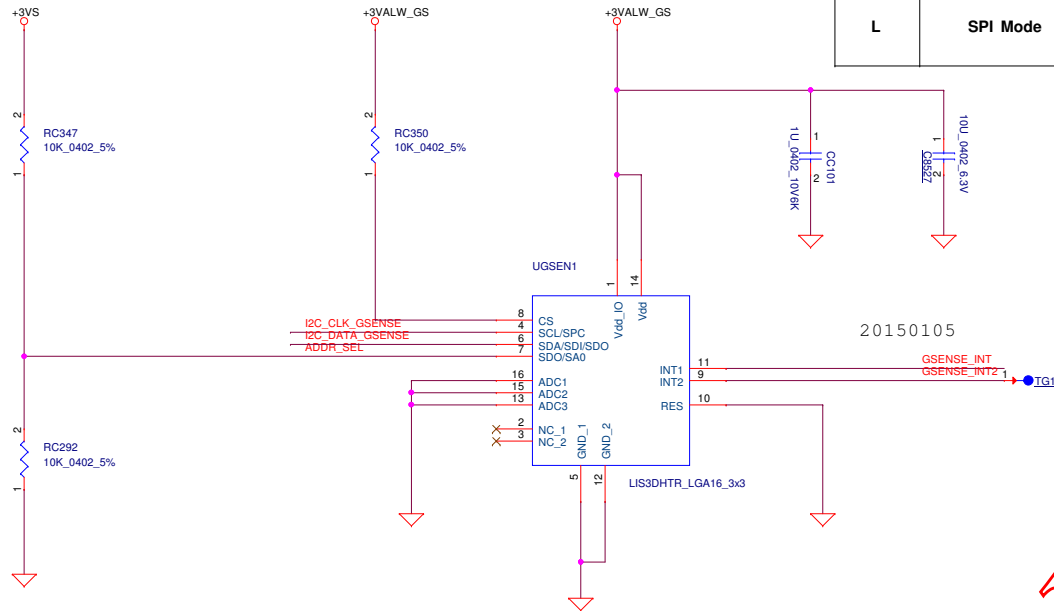


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

APS G-Sensor

TABLE

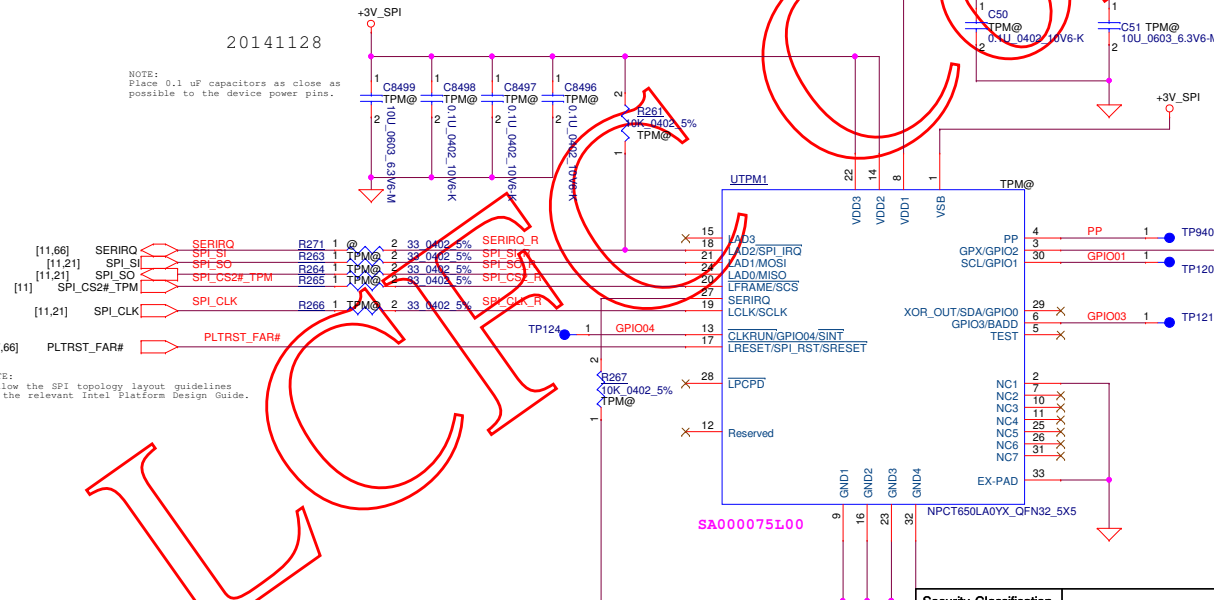
P/N	Mode Selection
H	I2C Mode
L	SPI Mode



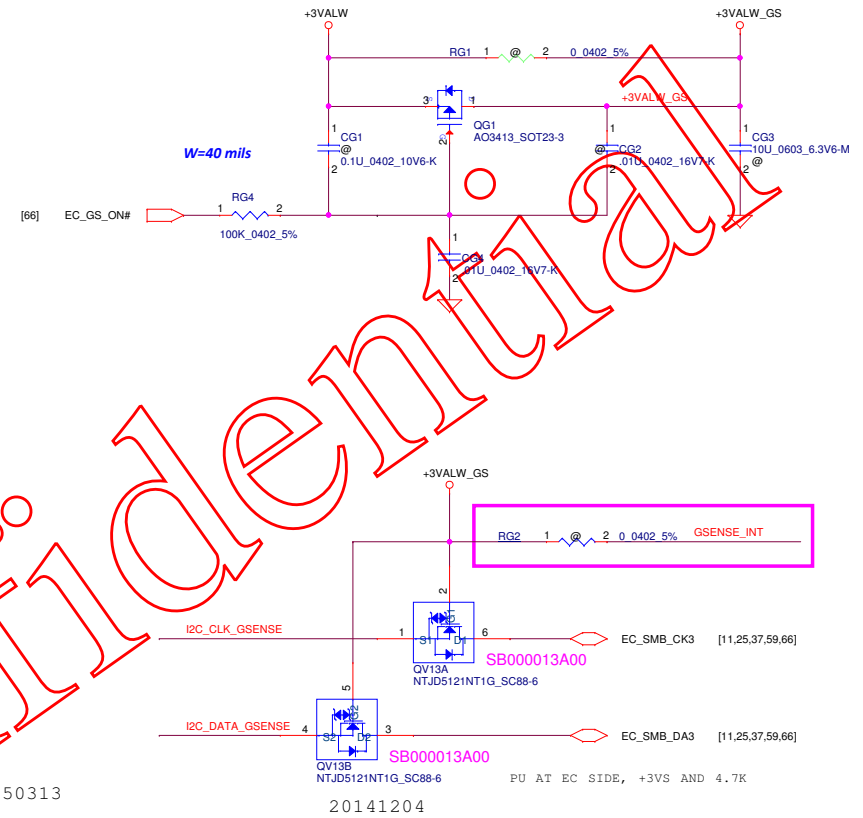
Only for UMA SKU

20141128

NOTE:
Place 0.1 uF capacitors as close as possible to the device power pins.



NOTE:
Follow the SPI topology layout guidelines in the relevant Intel Platform Design Guide.



TABLE


P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
LIS3DH	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
KX023-1025	L	3Ch (W) & 3Dh (R)

	Q29	R268	R273	R9456
New silicon NPCT650LA0YX	X	O	X	X
Current silicon NPCT650LA0YX	O	X	O	O


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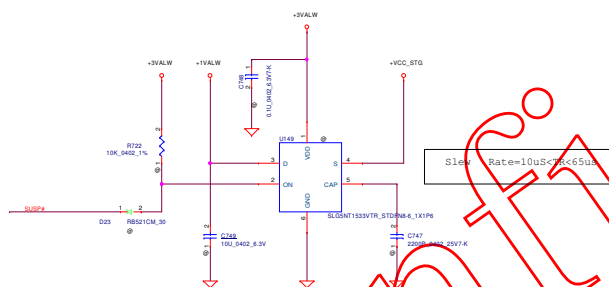
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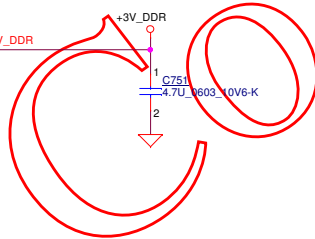
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LCEC

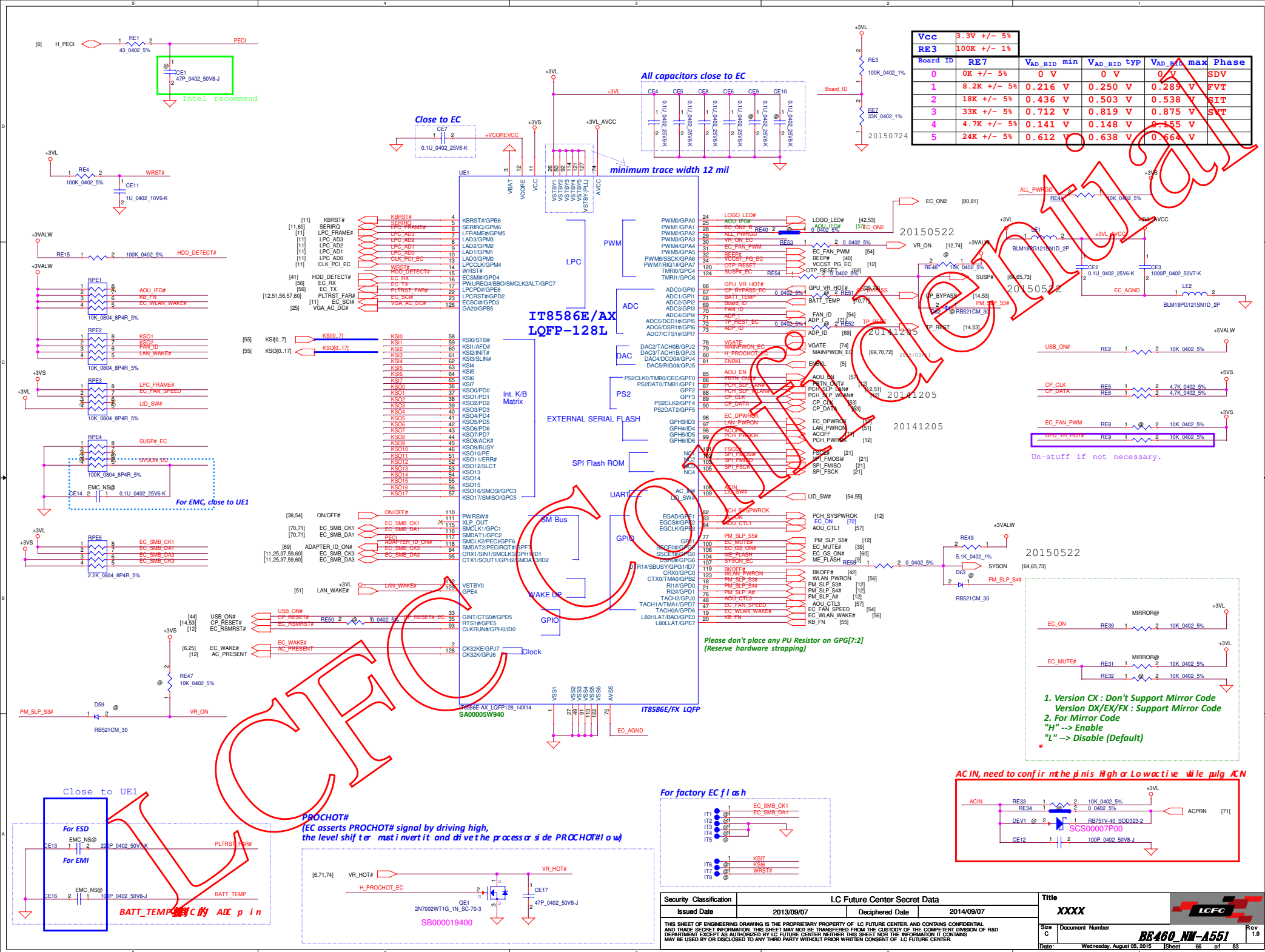


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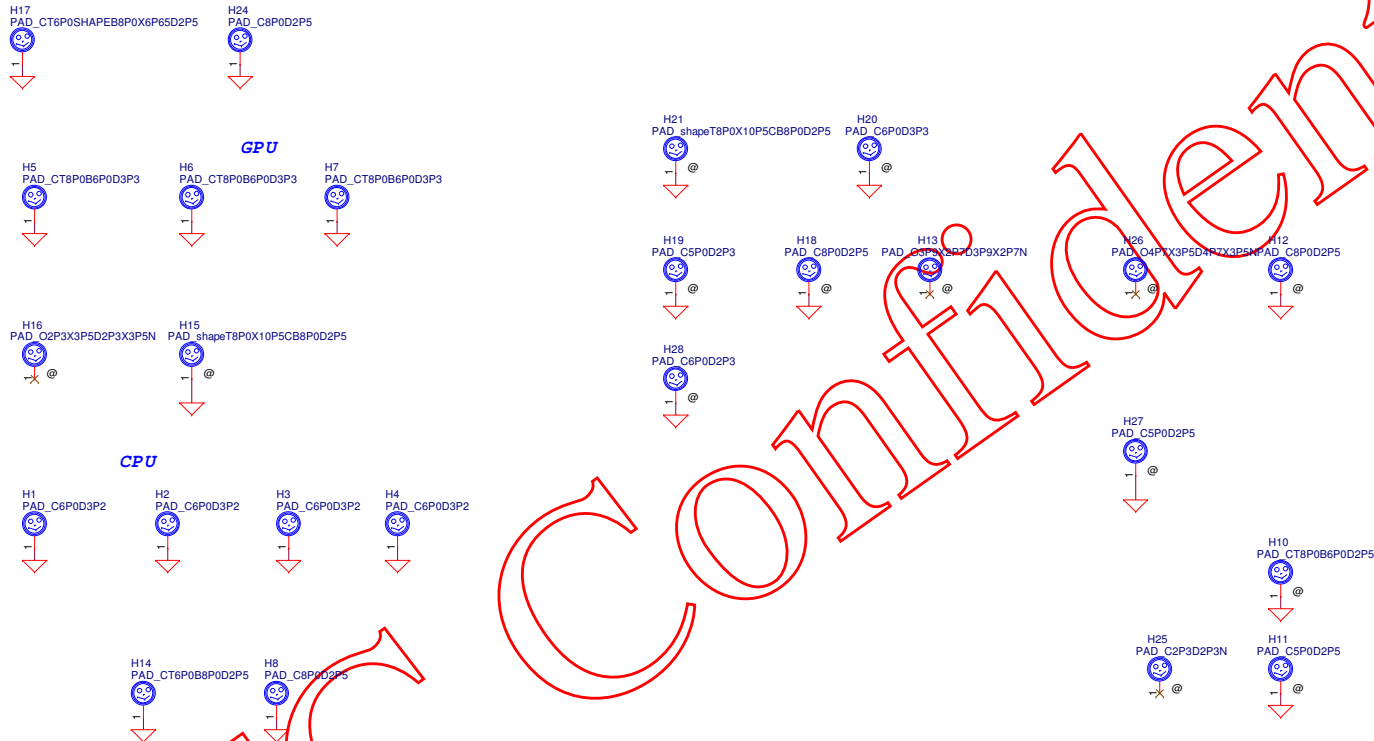
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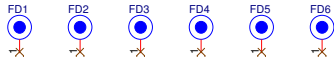
Screw Hole





CPU


GPU

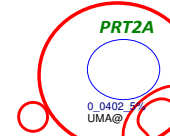
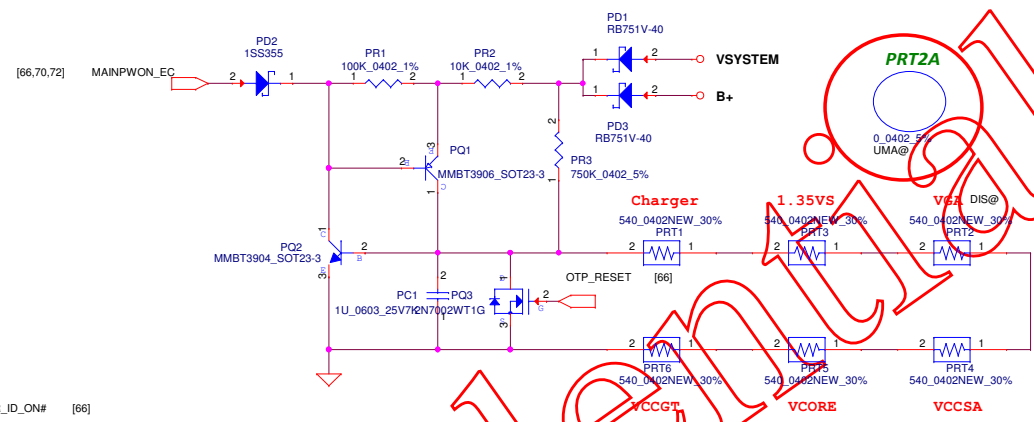
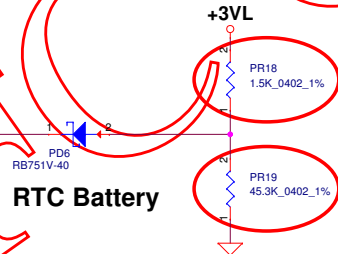
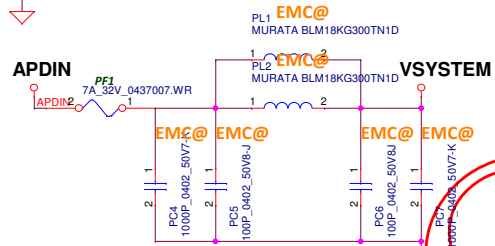
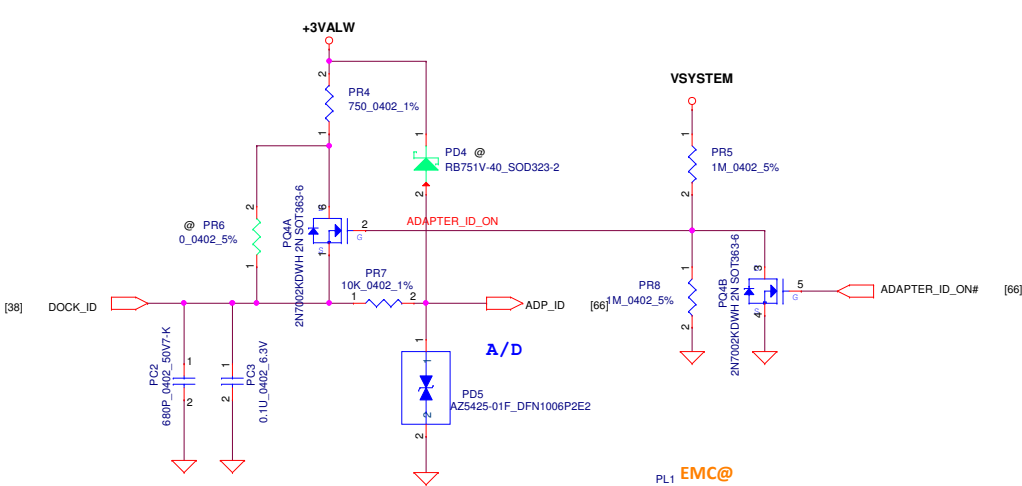
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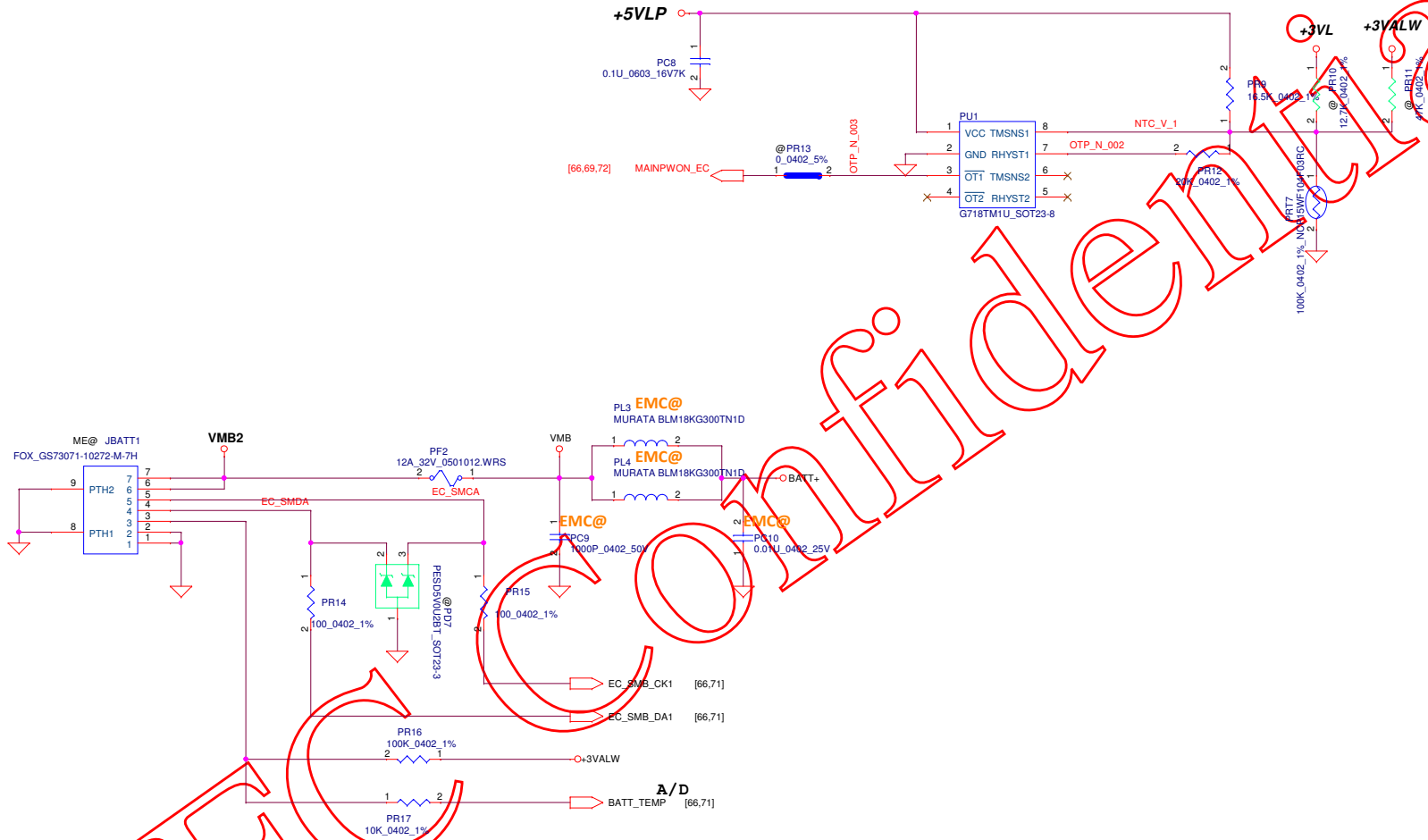
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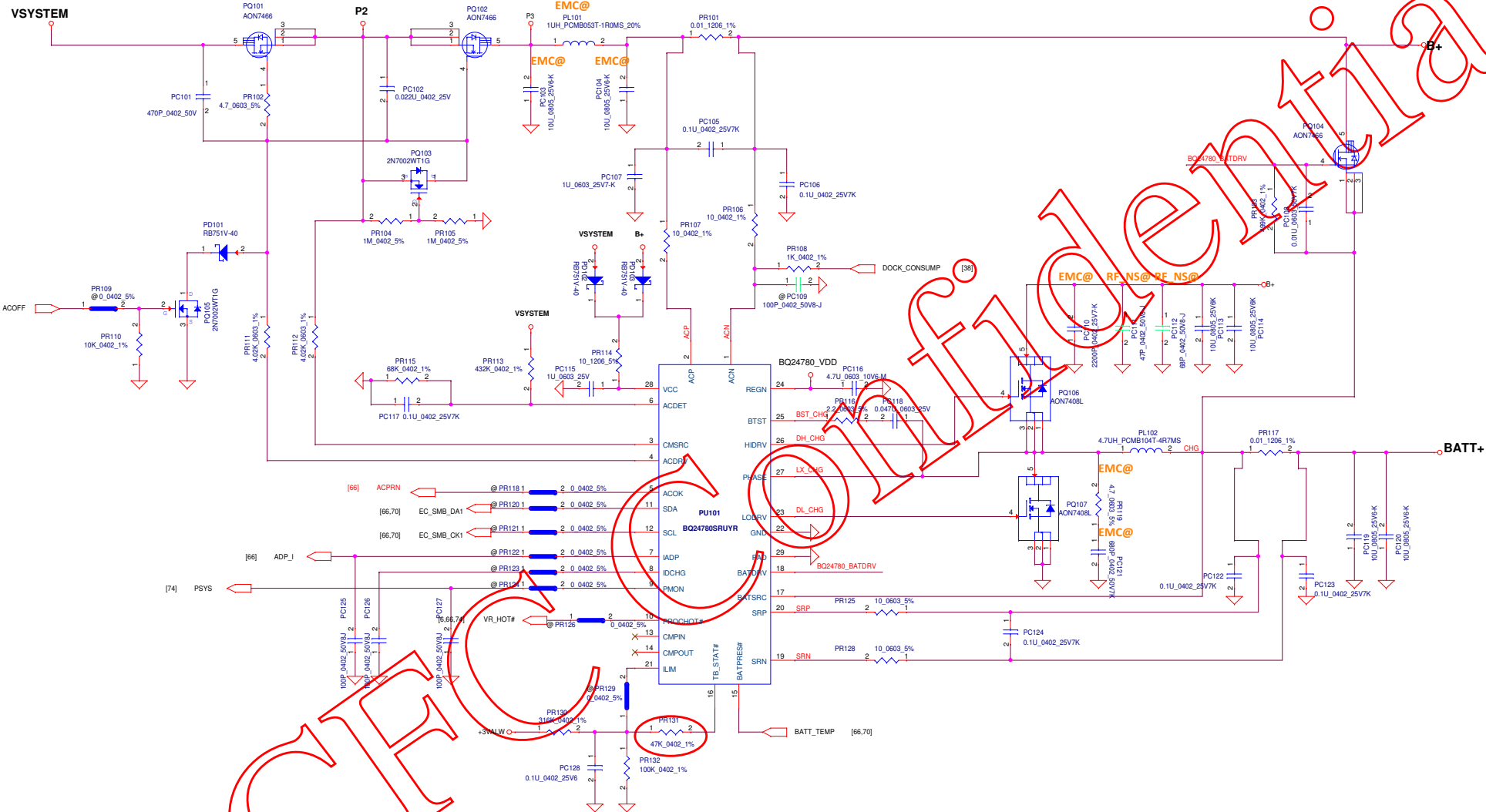
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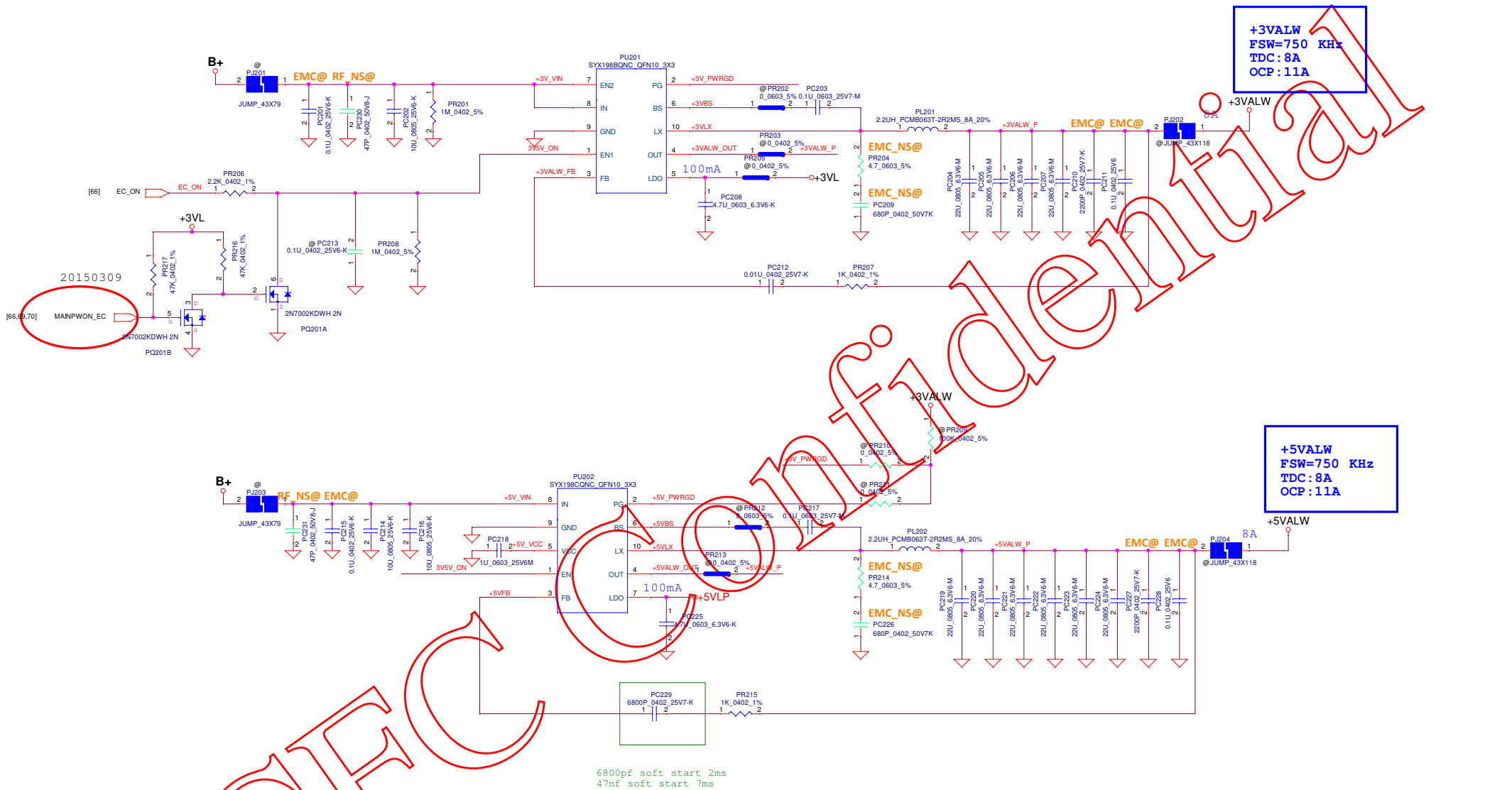
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PRT7 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

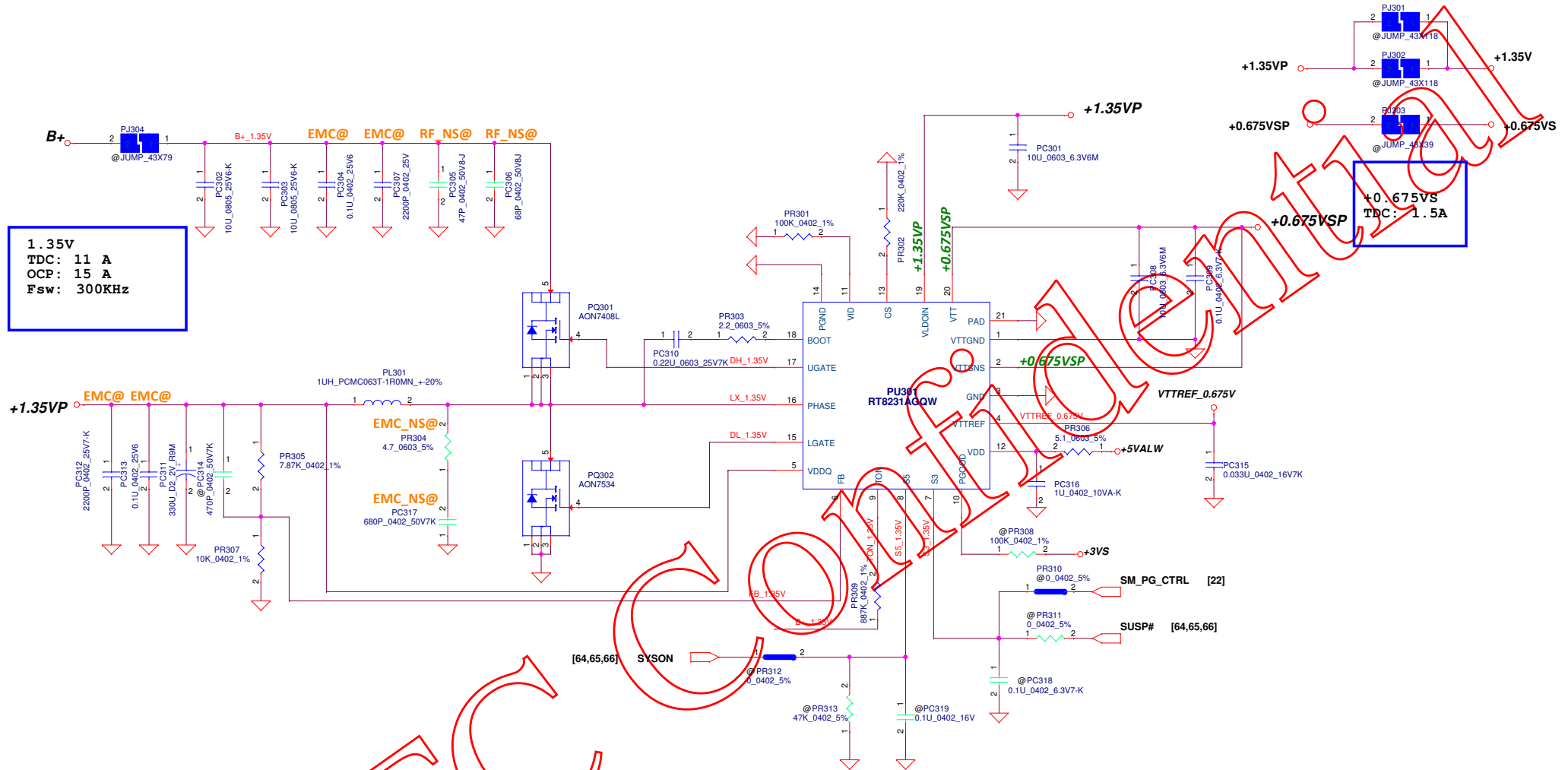


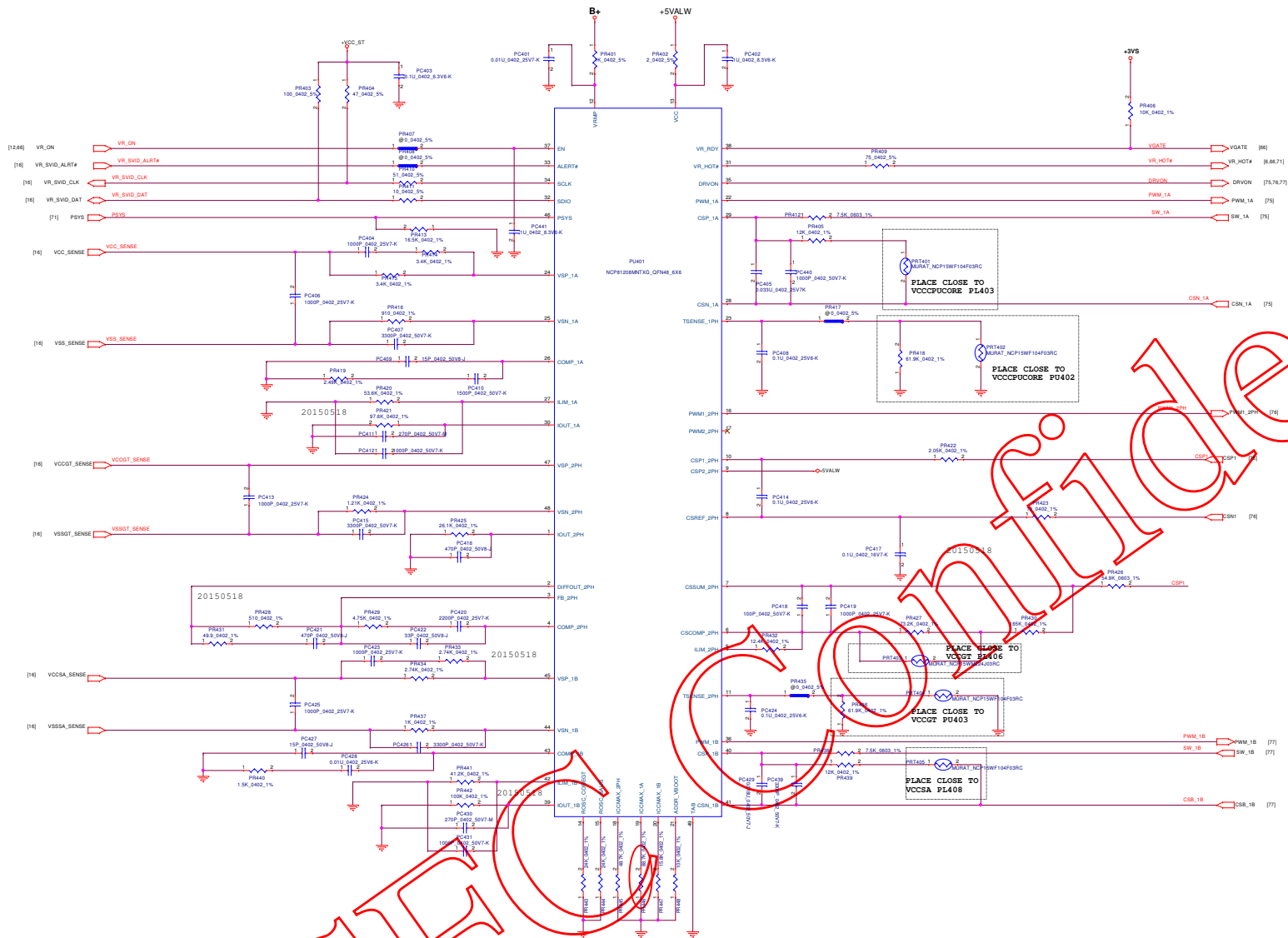
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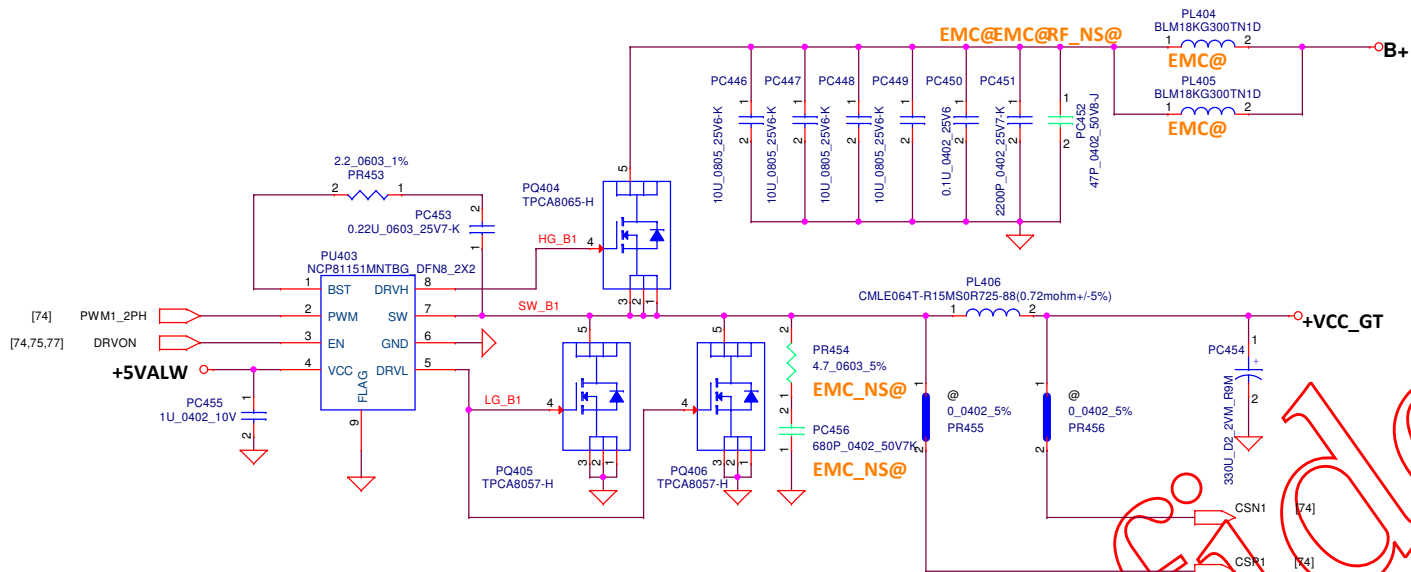




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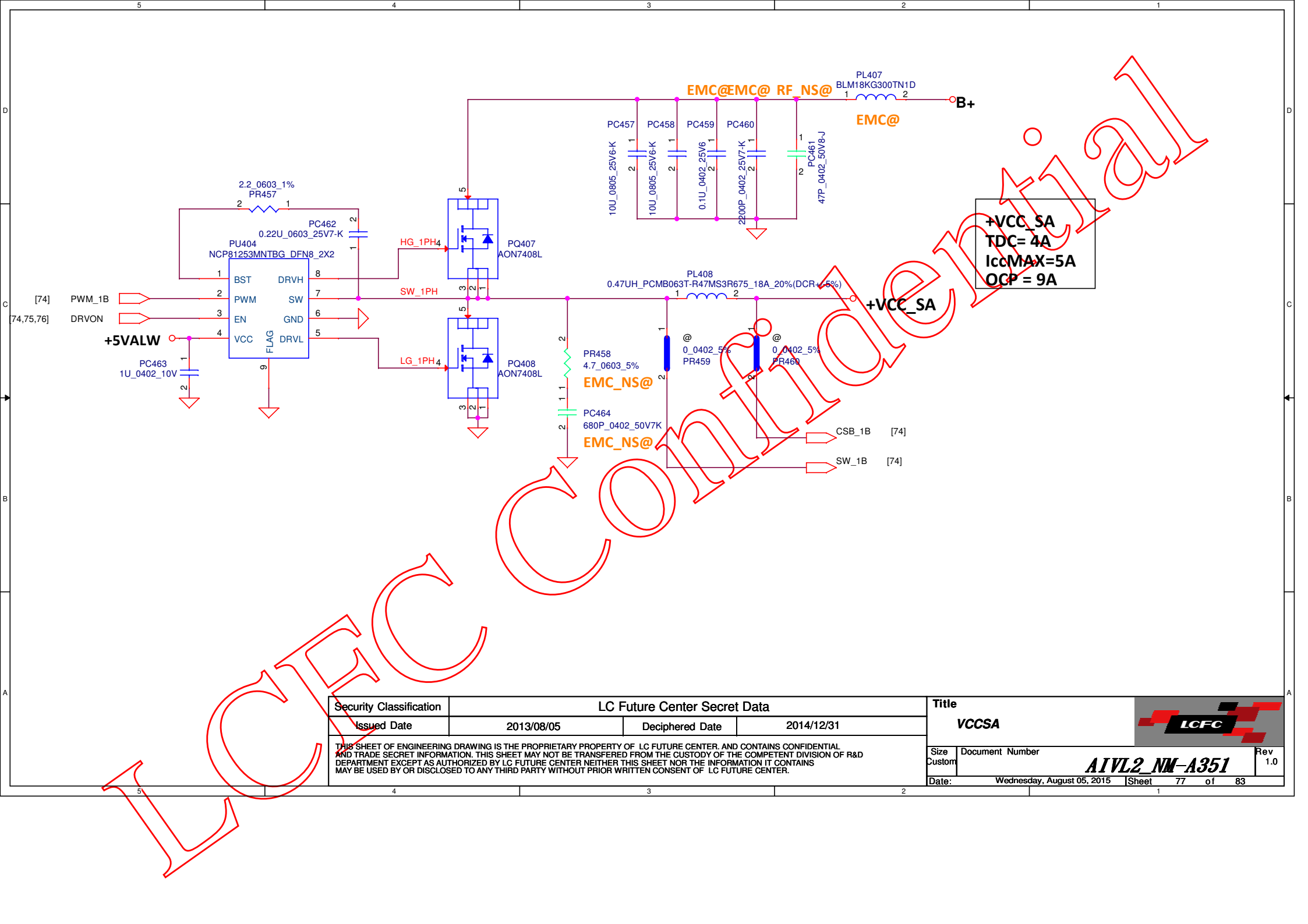
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IccMAX=31A
OCP min = 40A


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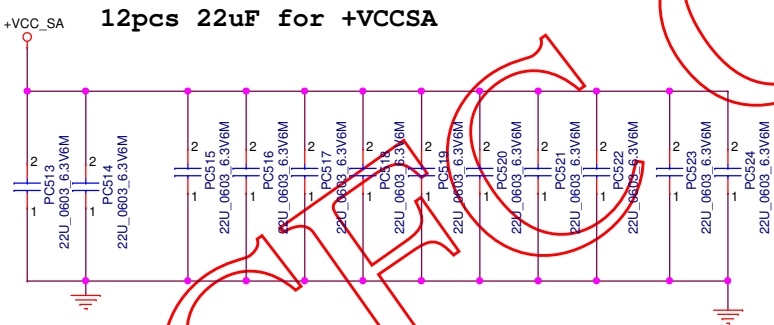
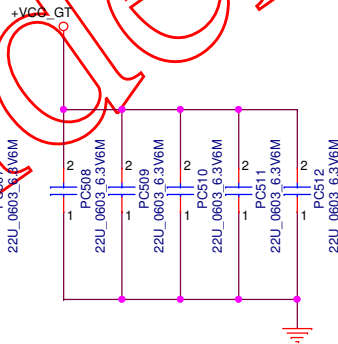
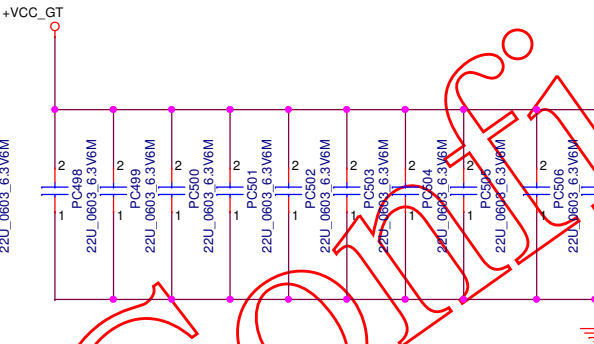
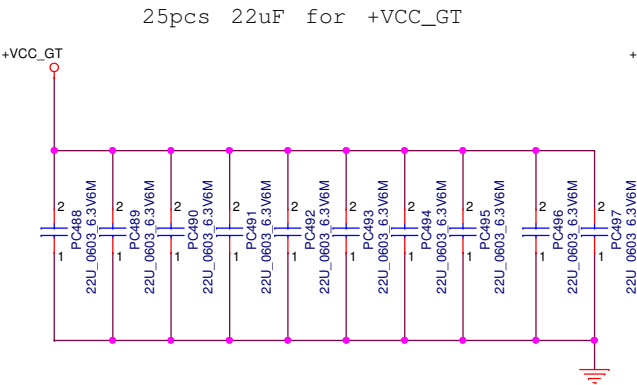
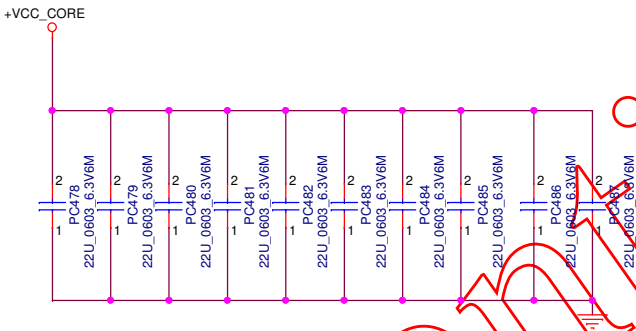
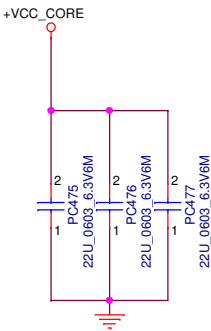
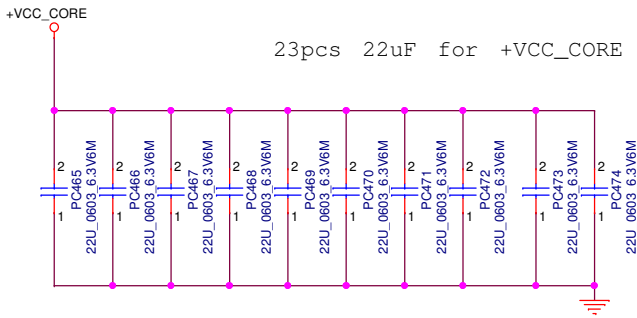
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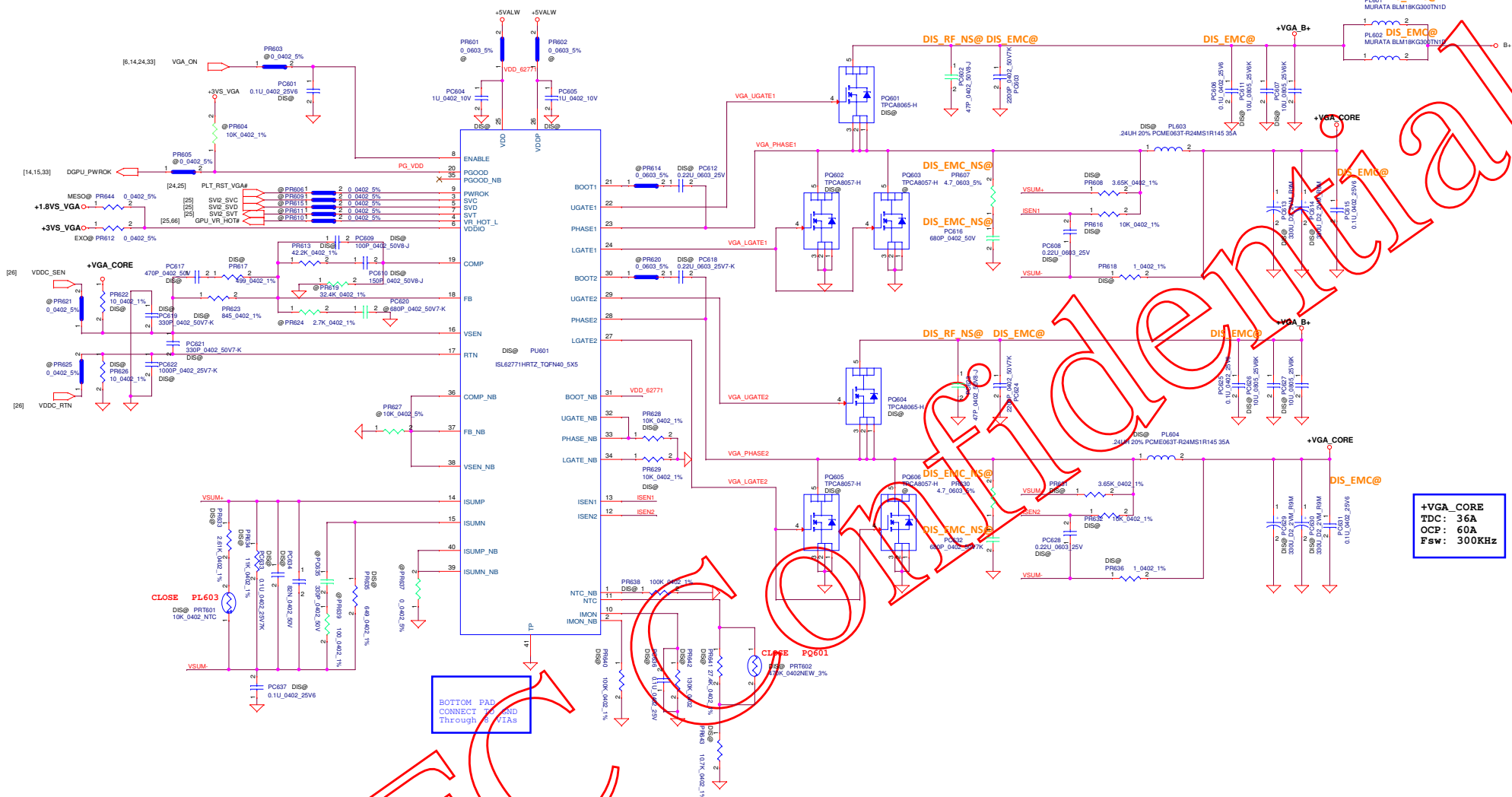
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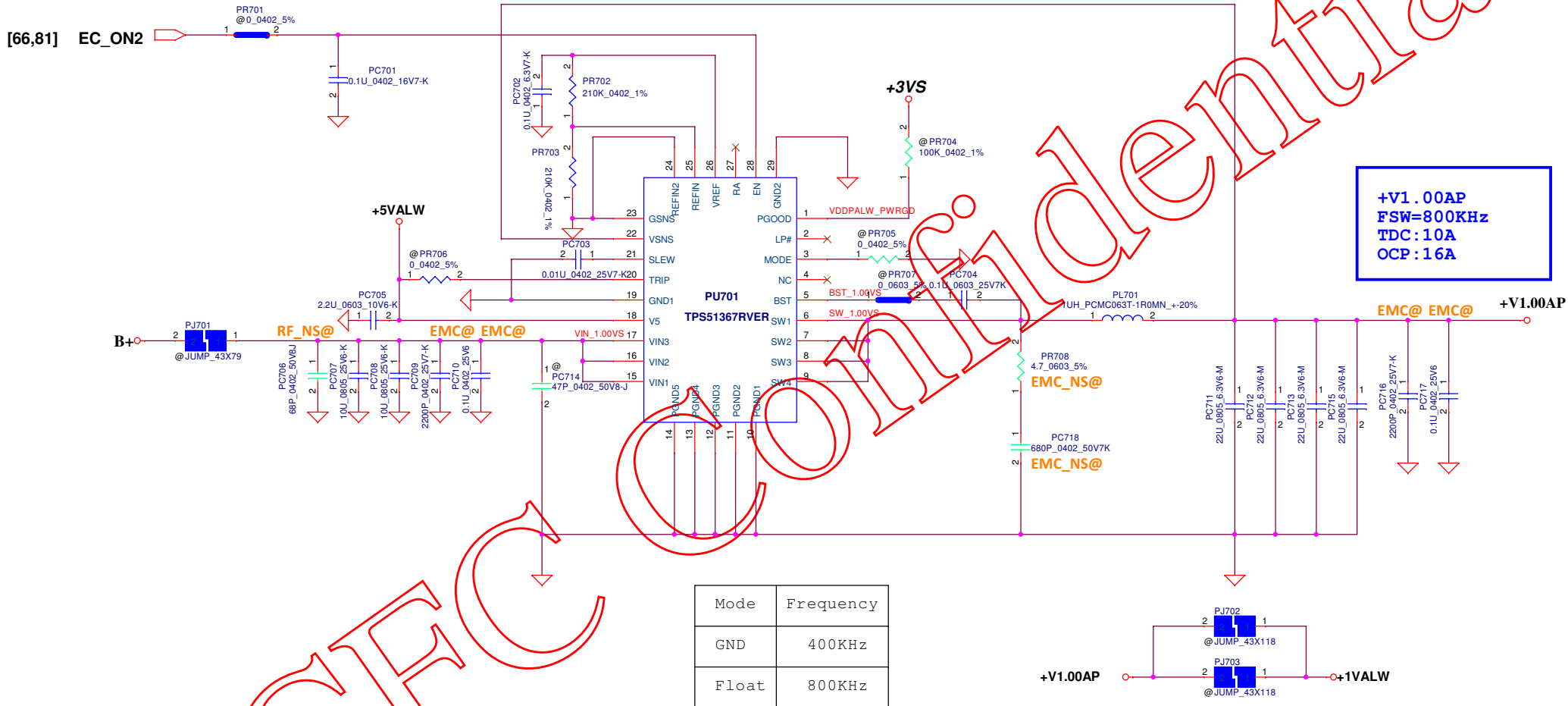
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ISL62771 Schematic for FT3 solution



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HW PIR (Product Improve Record)

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REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/10/15

NO DATE PAGE MODIFICATION LIST PURPOSE

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